A Wideband Bandpass Sigma-Delta Modulator for Wireless Applications*

Ali Tabatabaei and Bruce A. Wooley

Center for Integrated Systems
Stanford University
Stanford, CA 94305

Introduction

The increasingly complex modulation and compression algorithms employed for wireless communications have dictated the extensive use of digital signal processing in such systems. Moreover, the extensive use of digital signal processing promises to enable the realization of agile, programmable transceivers that can be adapted to meet a variety of standards.

The early digitization of signals in a radio receiver offers a number of potentially significant benefits, including reduced sensitivity to analog circuit imperfections, few off-chip components, and the ability to aggressively exploit the scaling of VLSI technology. However, as the digital signal processing is moved closer to the receiving antenna, the demands on the speed and dynamic range of the analog-to-digital converter become increasingly severe.

This work introduces a two-path, sixth-order, switched-capacitor sigma-delta modulator capable of digitizing a 1.25-MHz signal band centered at an IF of 20 MHz. The modulator samples the input at 80 MHz and implements its constituent resonators by chopping the signal at the IF ($f_S/4$). It thus also acts to demodulate the I and Q components of the signal and mix them to baseband. An experimental prototype of the modulator has been implemented in a 0.25-μm CMOS technology and shown to provide a dynamic range of 80 dB when operated from a single 2.5-V supply.

Architecture

Bandpass oversampling modulators have been shown to be an effective means of digitizing radio signals at intermediate frequencies as high has 20 MHz [1]. However, previously reported designs have been limited to bandwidths of at most 200 kHz if they are to achieve the dynamic range required in typical wireless receiver applications. To meet the dynamic range and bandwidth required in systems based on standards such as IS-95 CDMA, a means must be found to increase the attainable dynamic range at a relatively low oversampling ratio.

Fig. 1 shows a proposed modulator architecture that achieves high in-band noise suppression at low oversampling ratios through the use of third-order noise shaping and a multibit quantizer. Noise suppression and linearity comparable to those of a cascaded 4-2 bandpass topology are obtained while employing only a single 4-bit quantizer. In this architecture, the multibit quantized output is fed back around the third resonator so as to ensure the modulator's stability and decorrelate the quantization noise of the 1-bit quantizer formed by the MSB from the input [2]. As in the case of cascaded modulators with multibit quantization in the final stage, nonlinearity in the multibit DAC is suppressed by the second-order noise shaping provided by the first two resonators.

The architecture in Fig. 1 can be partitioned into two interleaved paths, each sampling at half the overall sampling rate, with the resonators replaced by high-pass filters [1]. Shown in Fig. 2 are two alternative implementations of the high-pass filters. Because of the feedback around the integrator the first implementation suffers from an increased sensitivity to additive noise at the output of the integrator. The second implementation achieves an equivalent response by chopping the input and output of the integrator at the IF, which corresponds to half the sampling frequency of each interleaved path. Fig. 3 illustrates the architecture that results from substituting the second filter implementation into the architecture of Fig. 1.

As can be inferred from Fig. 3, the mixer at the output of a resonator can be combined with the mixer at the input of the next resonator. Such a modification reduces the number of mixers to two, one at the input and the other one at the output of the modulator. The output mixer can also be eliminated since the input mixer serves to demodulate the I and Q components and down convert them to baseband. There is no need for up conversion.

The final architecture employing a single mixer at the input of each path is shown in Fig. 4. Two identical paths are employed to digitize the quadrature components of the bandpass input signal.

Circuit Implementation

The input mixer simply alternates the polarity of the input and can be implemented with MOS switches [3]. The input mixer and the first integrator are shown in Fig 5, while the clock phases for this circuit are depicted in Fig 6. The 180° phase shift between Φ1 and Φ2 is realized by passing a double-frequency input clock through a frequency divider. Therefore, all clock phases are derived from a single reference to achieve low systematic phase error and minimal sensitivity to duty cycle. A folded cascode op amp with a gain of 60 dB is used to implement the integrators. The total power consumed

* This research was supported by the NSF under contract MIP-9710647 and by National Semiconductor Corp.

by the modulator is 90 mW. The analog switched-capacitor circuits consume 62 mW, more than half of which is dissipated in the first integrators. The settling time for each integrator is about 11τ, where τ is the integrator time constant.

Fig. 7 shows the measured SNDR for the modulator. Clock jitter is believed to limit the SNDR at high signal levels. The measured output spectrum over the signal band is shown in Fig. 8. The mirror image that results from the mismatch between the two paths is suppressed by 53 dB. The prototype chip has an active area of 0.9 mm^2.

Acknowledgment

The authors gratefully acknowledge S. Chin, P. Tucci and the National Semiconductor Corp. for their guidance and support. They are also indebted to A. Ong, S. Rabii and D. Su for their assistance in the design and fabrication of the prototype.

References

[1] A. K. Ong and B. A. Wooley, "A Two-Path Bandpass ΣΔ Modulator for Digital IF Extraction at 20 MHz," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1920-1934, Dec. 1997.

[2] A. Hairapetian and G. C. Temes, "A Dual-Quantization Multi–Bit Sigma Delta Analog/Digital Converter," *IEEE Symp. on Circuits and Systems*, vol. 5, pp. 437-440, 1994.

[3] B. S. Song, "A Fourth-Order Bandpass Delta-Sigma Modulator with Reduced Number of Op Amps," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1309-1315, Dec. 1995.

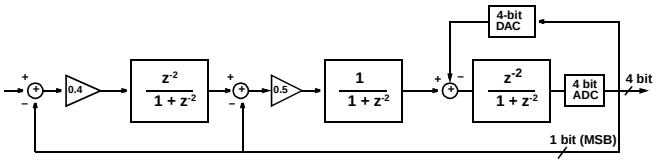

Fig. 1. Proposed architecture.

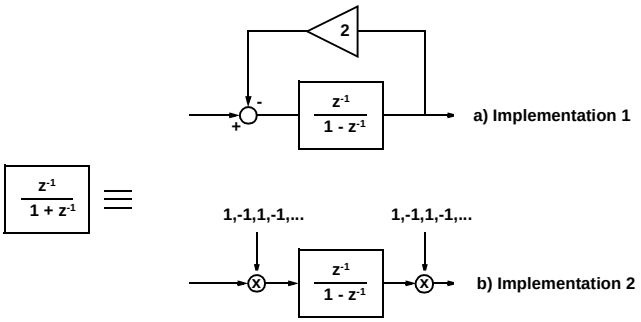

Fig. 2. High-pass filter implementations.

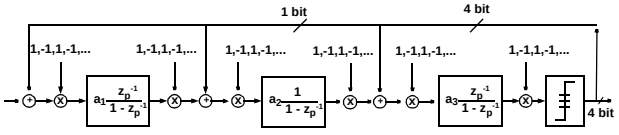

Fig. 3. Resonator substituted architecture.

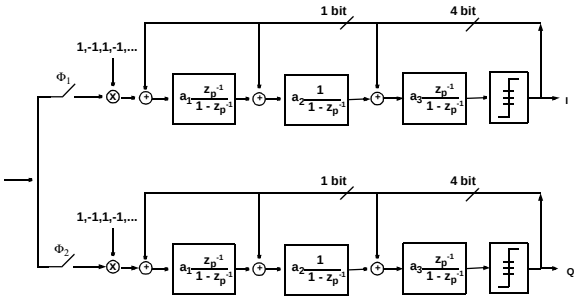

Fig. 4. Complete two-path architecture.

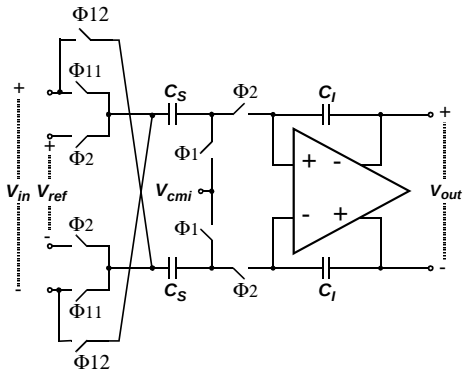

Fig. 5. Mixer and first integrator.

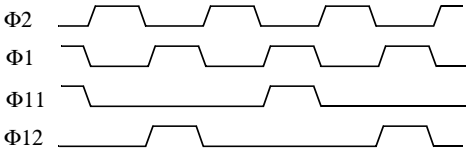

Fig. 6. Clock phases.

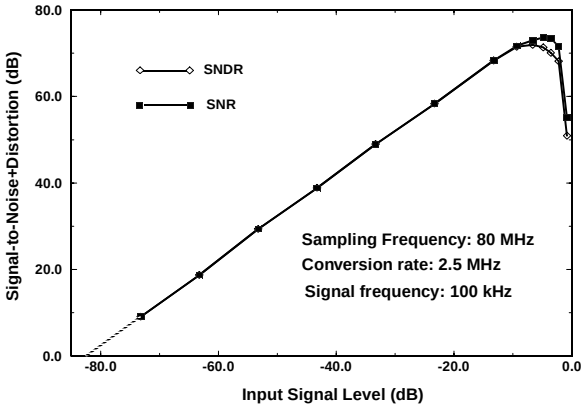

Fig. 7. Measured SNDR.

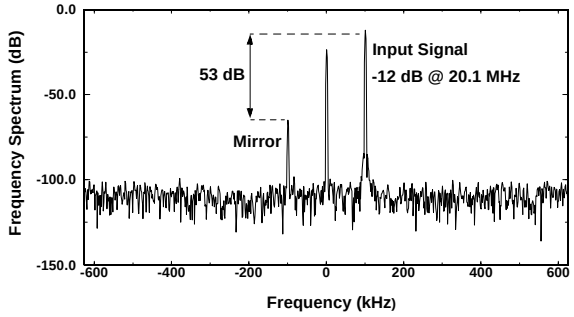

Fig. 8. Complex frequency spectrum