Abstract

Emerging wireless communications infrastructures employ increasingly complex algorithms and protocols to optimize the use of bandwidth, minimize cost, and enhance the portability of wireless personal communication systems. A majority of modern telecommunication protocols require that the transmitter power be adjustable over a wide range. This feature, commonly referred to as power control, ensures that an adequate signal is received by the base station, while conserving power and reducing the potential interference in other channels by lowering the transmitted power when the maximum transmitted power is not required. Many wireless networks require that the transmitted power be adjustable over a range as wide as 20 dB.

This dissertation investigates various architectures and concepts for the design and control of radio-frequency (RF) power amplifiers. The merits and challenges of integrating RF power amplifiers in CMOS technology are discussed, and a number of RF power amplifier performance metrics are introduced. Various power amplifier topologies are then reviewed, followed by a description of approaches and architectures for the control and linearization of these amplifiers. Finally, to address efficiency degradation in systems using power control, a novel parallel amplifier architecture is proposed.

A CMOS RF power amplifier introduced in this dissertation uses parallel amplification to provide high efficiency over a broad range of output power. Three binary-weighted class F unit amplifiers act in conjunction with an efficient power combination network to provide a digital-to-analog conversion between a 3-b control signal and the amplitude of the output RF signal. The power combination network is based on quarter-wavelength transmission lines that also serve as class F harmonic terminations.

An experimental prototype of the parallel amplifier architecture, integrated in a 0.25-μm CMOS technology, occupies an active die area of 0.43 μm^2, operates at 1.4 GHz from a 1.5 V supply and provides an output power adjustment range of 7 mW to 304 mW. The amplifier achieves a maximum power-added-efficiency (PAE) of 49% and maintains a PAE of greater than 43% over 70% of its power range.