WA 20.5 A Two-Path Bandpass ΣΔ Modulator with Extended Noise Shaping*

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The proliferation of communications applications stimulates interest in digitizing bandpass signals with bandwidths of several MHz at intermediate frequencies above 10MHz. This multistage oversampling modulator combines lowpass and bandpass stages to achieve an extended dynamic range at low oversampling ratios. An experimental prototype of the architecture integrated in 0.25μm CMOS achieves 75dB dynamic range for 2MHz signal bandwidth at 16MHz IF.

Oversampling modulators are an effective means of digitizing signals with a large dynamic range without precise matching of analog circuits components. However, the fundamental benefits of these converters generally derive from the ability to achieve a large oversampling ratio. In applications where the oversampling ratio is constrained by technology limitations or power considerations, multiple cascaded stages are commonly used to increase the modulator order and thus reduce the oversampling ratio needed to achieve a given dynamic range.

In a cascaded, or multistage, ΣΔ modulator, each stage following the first is designed to cancel the quantization noise of the preceding stage. In a conventional architecture, all of the stages are themselves oversampled, with the null in their noise shaping placed at the center of the signal band. Thus, the noise cancellation is most effective at the center of the signal band, and the density of the quantization noise in the modulator output increases from the center to the edges of the signal band, as depicted in Figure 20.5.1a. As the quantization noise is progressively shifted toward the band edges in the cascade, additional stages contribute progressively less to increasing the overall dynamic range.

Alternatively, quantization noise at the edges of the signal band can be cancelled more efficiently by altering the noise shaping in the later stages of a cascade. Figure 20.5.1b illustrates how moving the null in such stages to the band edges can attenuate the noise where its energy is the largest. As implied by Figure 20.5.1b, a bandpass modulator stage with its null shifted to the band edge can be used for this purpose. In this work, such an approach is adopted to extend the dynamic range of the bandpass ΣΔ modulator shown in Figure 20.5.2.

In the architecture of Figure 20.5.2, a bandpass signal is digitized by first shifting the I and Q components of the signal to baseband and then digitizing these signals with two parallel low pass modulators that are clocked at one-half the sampling frequency of the overall modulator [1]. Each of the lowpass modulators is then implemented with the three-stage architecture shown in Figure 20.5.3. Conventional 1b, 2nd-order low-pass ΣΔ modulators are used as the building blocks in this architecture.

In the three-stage modulator of Figure 20.5.3, the first two stages are simply low-pass ΣΔ modulators. In the third stage, the null in the noise shaping is shifted from dc to the band edge by means of a 4th-order bandpass modulator stage. Thus, the overall architecture, described here as a 2(LP)-2(LP)-4(BP) cascade, places two second-order notches at dc and one second-order notch at each end of the signal band. Simulations indicate that, when limited only by quantization noise, this architecture achieves 104dB dynamic range at an oversampling ratio of 16. They also show that the dynamic range would be reduced to 90dB by a 0.5% mismatch between analog and digital coefficients, including the sinusoidal coefficients in the mixers.

To implement the bandpass noise-shaping function in the third-stage of the lowpass modulator, the input to that stage is first mixed in quadrature so as to shift the noise shaping null from dc to the edges of the signal band. The required frequency shift is $f_s/(4M)$, where M is the oversampling ratio and fs is the sampling frequency for the overall modulator. The resulting I and Q outputs of this stage must be mixed back to their original frequency as part of the subsequent digital signal processing that combines the outputs of the three stages so as to suppress the quantization noise of the first two stages.

An implementation of the overall bandpass modulator of Figure 20.5.2, using the three-stage lowpass architecture of Figure 20.5.3, is shown in Figure 20.5.4. In the experimental prototype, a 16MHz IF input signal with 2MHz bandwidth is sampled at 64MSample/s. The front-end mixer down-converts the $f_s/4$ IF signal by alternating the polarity of consecutive samples, which is readily accomplished with appropriate sampling switches at the modulator input [2]. No other analog circuitry is required.

The mixers at the input of the third stage in the lowpass modulator are switched-capacitor variable-gain amplifiers, as shown in Figure 20.5.5. Eight different capacitor values are used to weigh each sample with its corresponding sine coefficient. Folded-cascode amplifiers with a gain of at least 60dB gain are used to implement the mixer/integrator circuits.

The modulator of Figure 20.5.4 is integrated in a 0.25μm CMOS technology in an active area of 2.8mm^2. The circuit dissipates 140mW from a 2.5V supply. The analog switched-capacitor circuits disipate 100mW, and the clock generator circuits dissipate 10mW; the remaining 30mW is dissipated in the digital output drivers. A plot of measured SNDR vs. input signal level is shown in Figure 20.5.6. The modulator attains 75dB dynamic range and 70dB maximum SNDR. At present, the maximum sampling frequency for which this performance can be maintained is believed to be limited by noise coupling on the test board rather than by the circuit itself.

Figure 20.5.7 shows the measured complex output spectrum of the overall three-stage modulator, along with the spectrum obtained using only the outputs of the first two modulator stages. This comparison demonstrates that the third stage effectively cancels the quantization-noise at each end of the signal band. The dc component in the output of the modulator results from capacitor mismatch and amplifier offset in the first modulator stage. The 1MHz component is due to similar nonidealities in the third stage as the third-stage mixers up-convert the effect of these nonidealities from dc to 1MHz. However, these tones do not limit the dynamic range and can be removed by digital filtering.

Mismatch between I and Q paths of the overall modulator creates the mirror signal apparent in Figure 20.5.7. The mismatch is the result of both component mismatch and non-orthogonal sampling. The measured 40dB mirror-signal attenuation is acceptable for most communications applications.

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References:

[1] Song, B. S., "ΔA Fourth-Order Bandpass Delta-Sigma Modulator with Reduced Number of Op Amps," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1309-1315, Dec. 1995.

[2] Tabatabaei A. and B. A. Wooley, "A Wideband Bandpass Sigma-Delta Modulator for Wireless Applications," *IEEE Symp. on VLSI Circuits*, pp. 91-92, June 1999.

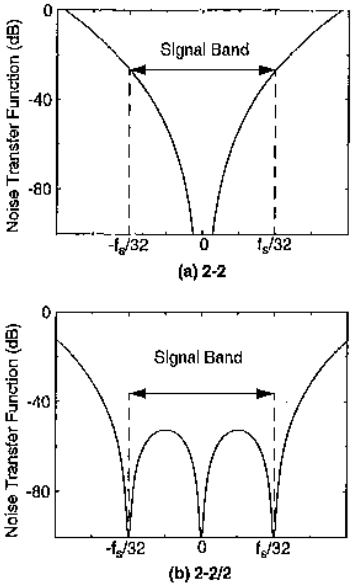

Figure 20.5.1: Noise transfer function for a two-stage modulator: a) Lowpass-Lowpass, b) Lowpass-Bandpass.

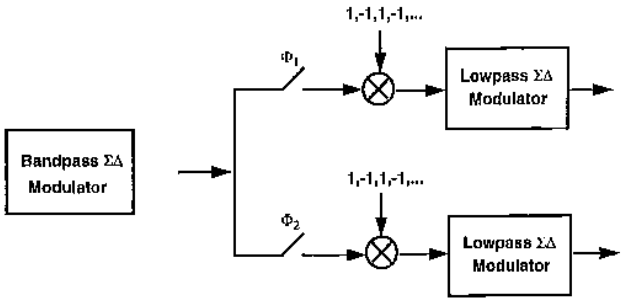

Figure 20.5.2: Implementation of a bandpass modulator.

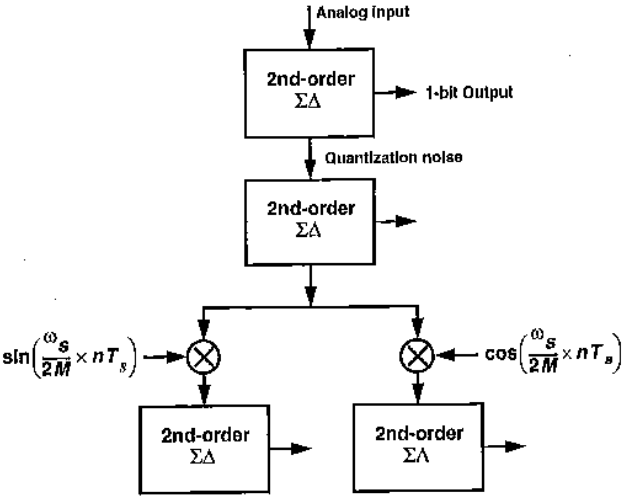

Figure 20.5.3: Three-stage lowpass modulator.

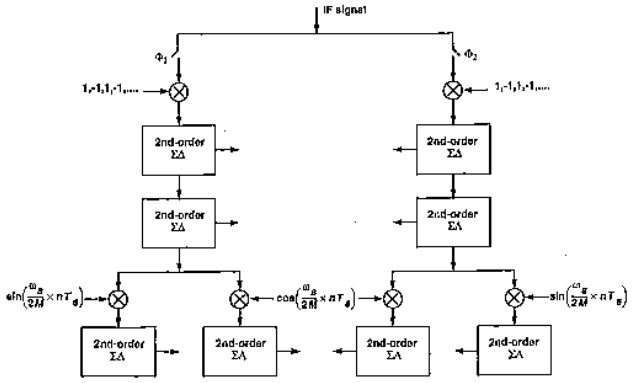

Figure 20.5.4: Bandpass modulator architecture.

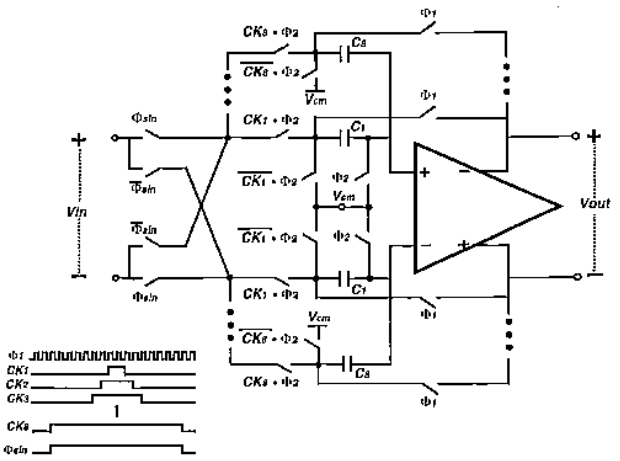

Figure 20.5.5: Third-stage mixer.

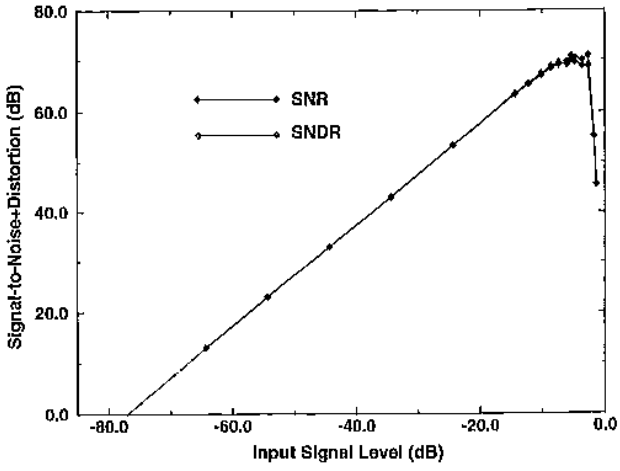

Figure 20.5.6: Measured SNR and SNDR.

Figure 20.5.7: See page 468.

Receivr Performance (RF=5.25 GHz, LO=5.26 GHz)

DSB Noise Figure	3 dB
Conversion Gain (50 Ω/1M Ω)	8.7/18 dB
Input S11	-9.4 dB
Input 1-dB compression	-21 dBm
IP2	16.1 dBm
IP3	-11.3 dBm
LO-RF Leakage	-60 dBm
Power Dissipation @ 3V	114 mW
Die Size	4 mm^2

Transmitter Performance (Baseband=150MHz, LO=5.55 GHz)

Output 1-dB compression @5.7 GHz	-2.5 dBm
Input 1-dB compression (peak, differential)	1.8 V/channel
LO Leakage	-22.4 dBc
Sideband Rejection	-33.4 dBc
Equivalent Phase Error	2.45 degree
Equivalent Amplitude Imbalance	0.4 dB
Power Dissipation @ 3V	120 mW
Die size	2.7 mm^2

Figure 19.2.8: Transceiver performance.

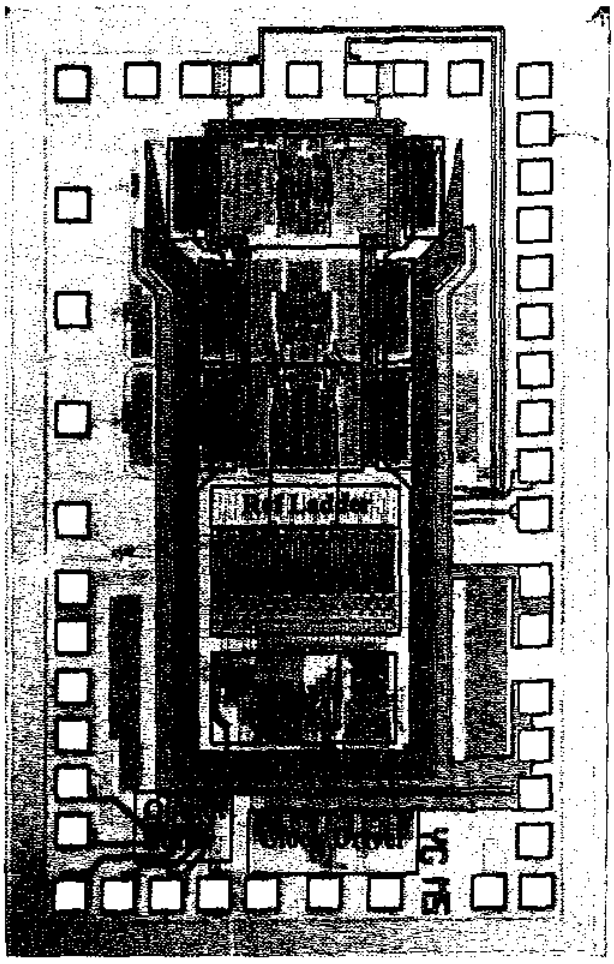

Figure 20.2.5: DS micrograph.

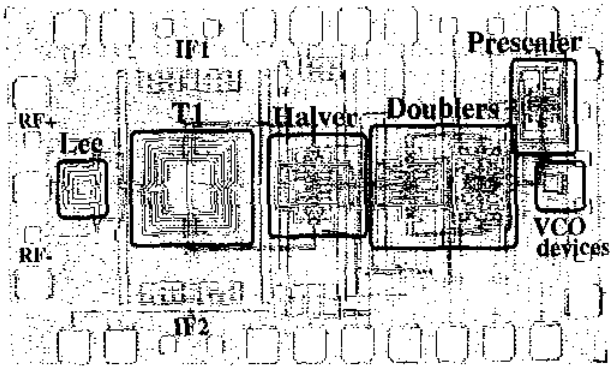

Figure 19.3.7: Chip micrograph.

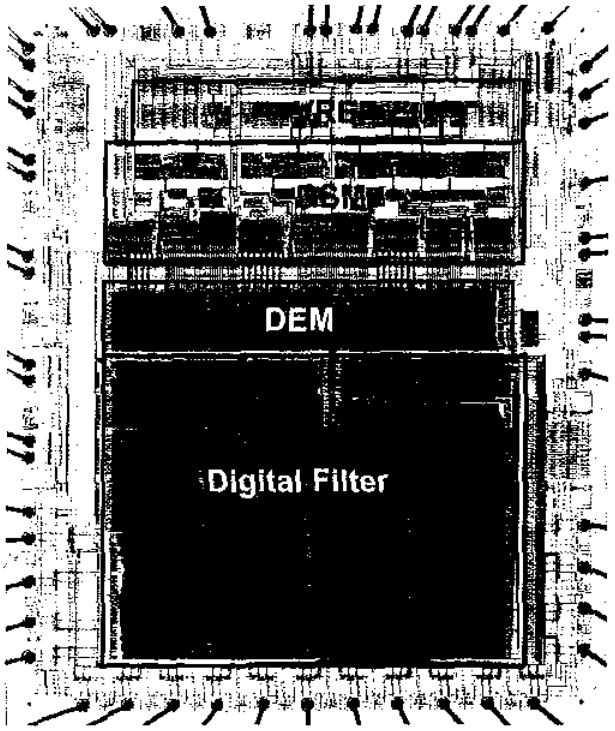

Figure 20.3.5: Chip micrograph.

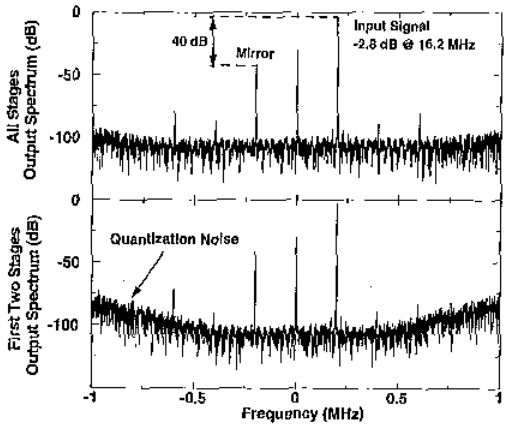

Figure 20.5.7: Measured output spectrum.

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