A 14-bit, 5-MHz Digital-to-Analog Converter Using Multi-bit ΣΔ Modulation*

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Abstract

A 14-bit D/A converter based on a pipelined fourth-order multi-bit sigma-delta modulator is presented. The 6-bit digital output of this modulator is converted to analog using current calibration. The converter achieves 85-dB dynamic range at 5-MHz signal bandwidth, using a single 2.5-V supply in 0.5-μm CMOS process.

Introduction

This work examines the application of sigma-delta (ΣΔ) techniques, traditionally used for high-precision low-frequency applications such as digital audio, to D/A conversion rates at above 2 MHz and resolutions exceeding 14 bits, with potential applications in data communications (VDSL,...).

The advantages of ΣΔ modulation include relaxed reconstruction filtering requirements and lower analog complexity. A single-bit modulator also benefits from the inherent linearity of its two-level analog output. A multi-bit modulator requires extra effort to linearize its multi-level output, but for the same loop order performs equally at a much lower oversampling ratio (OSR), which makes it more attractive for high-speed applications. As an example, a single-bit modulator requires an OSR>28 to achieve 14 bits of dynamic range, compared to an OSR=10 for a 6-bit modulator. Multi-bit modulators also have better immunity to instability and tones, and a lower out-of-band noise than their single-bit counterparts.

Among the techniques used to linearize the multi-bit output of a modulator, dynamic element matching (DEM) and current calibration are prevalent. DEM relies on oversampling to randomize the errors due to component mismatch. At OSR's of <12, however, this technique is not capable of generating 14+ bits from 10-bit component matching [1]. Current calibration has been shown to achieve 90dB of linearity at audio frequencies without relying on oversampling [2]. This paper presents a fourth-order modulator with 6-bit output using current calibration, achieving 14-bit dynamic range at a low OSR of 12.

Implementation

A. Digital Section

The block diagram of the fourth-order digital modulator is shown in Fig. 1. All multiplier coefficients are designed to be factors of 2, which greatly simplifies their implementation. These coefficients also guarantee stability over the entire range of the modulator input. High clock frequency of 120 MHz imposes strict requirements on the speed of the wide adders in series. Pipelining techniques were used to substantially reduce the design complexity by breaking down the wide adders into smaller ones. Fig. 2.(a) shows a sample 12-bit adder broken down into 4-bit adders using pipelining. In this design, the extra delay elements typically introduced by pipelining were mostly eliminated by using the existing delay elements inside the integrators as pipeline delays. Fig 2.(b) shows the basic building blocks used in implementing the modulator. The size of the adders in these blocks were chosen to meet the speed requirements for simple ripple carry adders in this 0.5-μm technology. Fig 2.(c) shows the highly modular final implementation of the modulator based on these building blocks.

The modulator generates 6 bits at 120 MHz. It achieves a dynamic range of 96 dB for a signal bandwidth of 5 MHz. The out-of-band noise is 36 dB below the maximum signal level.

B. Analog Section

The 6-bit modulator output is converted into a 64-bit thermometer code, which then generates the analog output using 63 identical current cells continuously calibrated to a reference current [2]. The current cell is shown in Fig. 3. During the calibration phase,† M2 is connected as an MOS diode through the feedback loop consisting of M6 and M7-M8, and the difference between I_{ref} and the coarse current source, M1 (designed to generate $0.97I_{ref}$), flows through M2, establishing a corresponding voltage on its large gate-source capacitance, C_{gs2}. In the normal operation phase, the charge stored on C_{gs2} forces the same current to flow through this transistor. Consequently, the overall current of the cell remains equal to I_{ref}.

M1 and M2 are cascoded to keep their drain-source voltage constant during operation. Transmission gates M9-M10 and M11-M12 are added to cancel the charge injection introduced by M7-M8 on C_{gs2}. M2 has a small transconductance to decrease the sensitivity of its current to small variations of its gate voltage. The high threshold voltages of the process, together with the low power supply of 2.5 V, dictated the large sizes of the transistors. The frequency of the calibration clock is 250KHz, corresponding to 4-μsec calibration time per current cell and 256μsec between consecutive calibrations for each cell.

Several precautions were taken to reduce the glitch energy in the output, including synchronization of the inputs to the 64 cells by using flip-flops and clock distribution trees, lowering the input swing of the diff-pair to decrease feedthrough, generating a high-crossing point for the diff-pair inputs to reduce the time both switches are in the off stage, and cascoding the current sources with a small transistor to decrease the capacitance on the common node of the diff-pair [3]. To fulfill the swing and crossing point requirements independent of the process, a special all-PMOS driver was designed as depicted in Fig. 4. The relative sizes of M1 and M4 determine the crossing point of the driver outputs. M2 and M3 were added to block the feedthrough of the inputs of the driver to its outputs. Three dummy branches were added to balance the load seen by the driver's inputs. The bias on the common line sets the driver's output swing to 0.8 V.

To reduce the effect of noise on the performance of the analog section, the gates of the current sources, as well as the digital power supply, were heavily decoupled to the GND [4]. Special care was taken to put ample substrate contacts around the current sources. The outputs are taken off chip differentially and drive a doubly-terminated 50-Ω line with a 0.5-V swing.

Experimental Results

The modulator was fabricated in a 0.5-μm CMOS technology. The chip operates from a single 2.5-V supply with 20mA analog current driving a doubly terminated 50-Ω transmission line. Fig. 5 shows the measured signal-to-noise ratio (SNR) and signal-to-(noise+distortion) ratio (SNDR) as functions of the input signal level for a 120-MHz sampling rate and an oversampling ratio of 12. These preliminary measurements demonstrate 85-dB dynamic range and 80-dB peak SNDR at a Nyquist conversion rate of 10 MHz.

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† An extra current cell is added to replace the cell under calibration.

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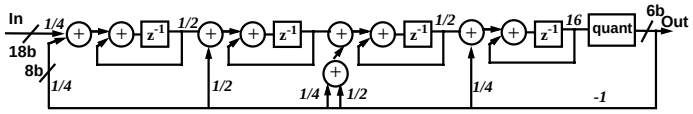

Fig. 1. Block diagram of the fourth-order digital modulator.

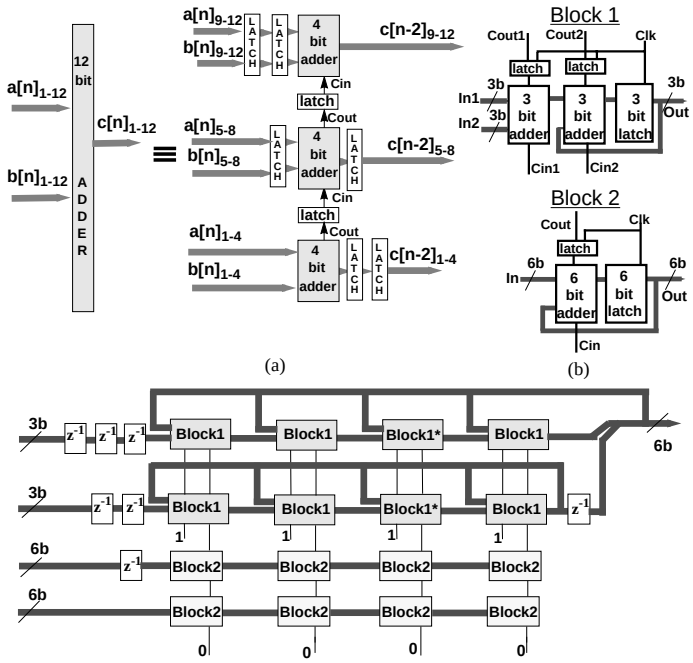

Fig. 2. (a) Pipelining a 12-bit adder (b) Building blocks of the digital modulator (c) Implementation of the modulator using the building blocks in (b).

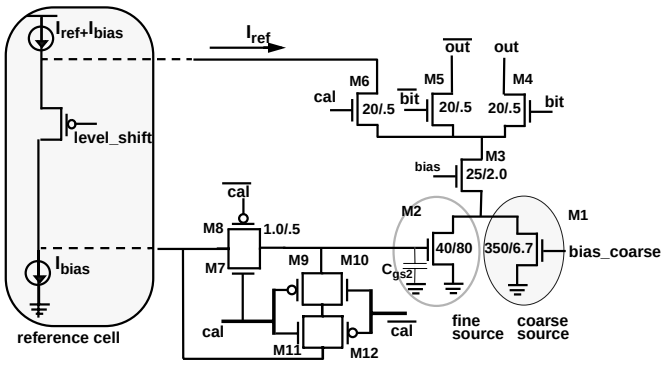

Fig. 3. Circuit schemetic of the current cell.

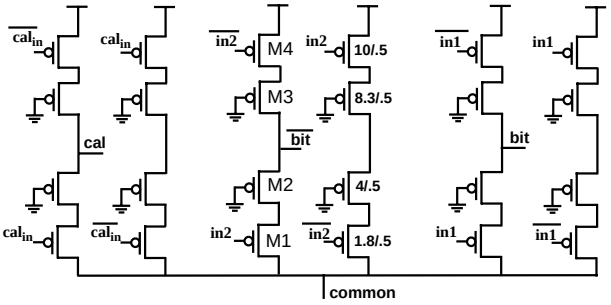

Fig. 4. Circuit schematic of the all-PMOS driver for the current cell.

Table 1. Performance summary

Supply Voltage	**2.5V**
Signal Bandwidth	**5MHz**
Sampling Frequency	**120MHz**
Oversampling Ratio	**12**
Dynamic Range	**85dB**
Peak SNDR	**80dB**
Power	
Digital	**25mW**
Analog	**75mW**
Area	
Modulator	**0.45mm^2**
Analog Section	**1.7mm^2**
Process	**0.5-μm CMOS**

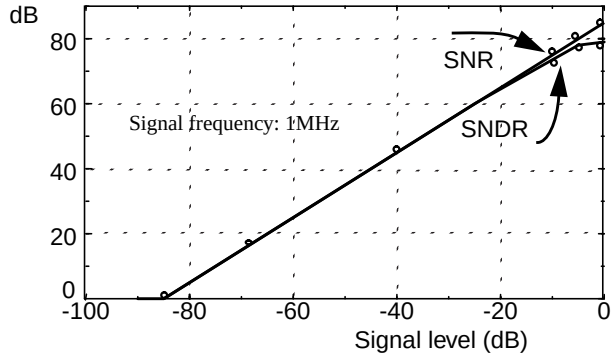

Fig 5. Measured SNR and SNDR vs. signal magnitude.

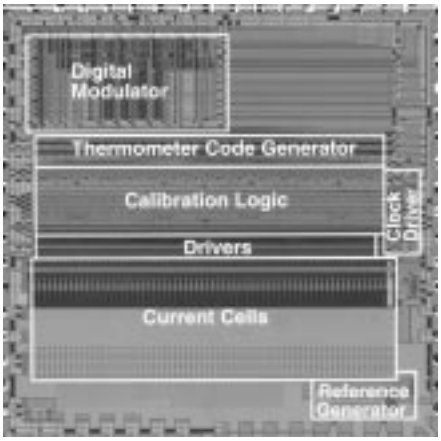

Fig. 6. Chip micrograph.