PER-PIXEL FLOATING-POINT A/D CONVERSION FOR HIGH-DYNAMIC RANGE, HIGH-FRAME RATE INFRARED FOCAL PLANE IMAGING

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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Infrared focal plane arrays (IR FPAs) have been widely used for medical, scientific, industrial, and military applications. These applications often require a high-frame rate (≥1000 fps) and high-dynamic range (≥19 bits) imaging to capture rapidly changing scenes at very high contrast. However, state-of-the-art FPAs with CMOS readout electronics and external high-speed A/D converters (ADCs) cannot meet these requirements because of the limited throughput of the analog readout and saturation of the integration capacitor that converts the IR detector current to a voltage signal. Several approaches to integrating ADCs with FPAs have been proposed to increase the throughput of the data conversion, and various dynamic range enhancement schemes have been developed to avoid integration capacitor saturation. However, limited power and area budgets for the IR FPAs have precluded the simultaneous use of these techniques.

By using three-dimensional integrated circuit (3-D IC) technology, IR FPAs can be integrated not only with conventional CMOS readout electronics, but also with ADCs and dynamic range enhancement schemes, to achieve both a high frame rate and a high dynamic range. In addition, the simultaneous optimization of the readout electronics, dynamic range enhancement, and ADC provides an opportunity to develop a new architecture that minimizes both power and area.

This dissertation introduces a per-pixel floating-point, dual-slope ADC architecture that achieves a high-frame rate and high-dynamic range IR FPA. Floating-point A/D conversion appears to be an alternate solution for uniform A/D conversion for low-power high-dynamic range data conversion. The proposed per-pixel ADC architecture achieves a high frame rate by removing the analog readout bottleneck between the IR detectors and external ADCs. Moreover, by adjusting the integration time of each pixel based on the detector current strength, the architecture attains a high dynamic range without much increase in power consumption. To improve the uniformity of the per-pixel ADC array, each ADC performs a unique analog offset cancellation combined with a digital correction.

Two experimental prototype arrays have been integrated. A prototype 16 x 16 ADC array integrated in a 0.18-μm CMOS technology achieves a 19-bit dynamic range and 8-bit mantissa resolution at 3000 fps, with a power consumption of only 7 μW/pixel. A second 16 x 16 ADC array integrated in a 3-D 0.18-μm FDSOI technology attains a similar performance; furthermore, each ADC partitioned into three layers successfully fits within a detector size of 50 x 50 μm^2, demonstrating A/D conversion using 3-D IC technology.

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Chapter 1 *Introduction*

1.1 Motivation

Infrared focal plane imaging arrays (IR FPAs) are widely used in industrial, scientific, medical, and military applications. In these applications, the demand for FPAs with a high frame rate (≥1 kHz) and a high dynamic range (DR) (≥19 bits) has been increasing to capture rapidly changing scenes at very high contrast. The current state-of-the-art IR FPAs, comprised of an IR photon detector array, per-pixel integration capacitors, and CMOS analog readout electronics with off-chip analog-to-digital converters (ADCs) [1], often cannot meet these emerging requirements because of the speed and the DR limitations of the CMOS readout electronics that interface the IR detector array and the external ADCs. The frame rate is limited primarily by the analog readout bottleneck, while the DR is limited by the saturation of the integration capacitor that converts the detector current into a proportional voltage.

Various dynamic range enhancement techniques have been developed to capture large dynamic range signals without saturating the capacitors on which the detector currents are integrated. To improve both the DR and the signal-to-photon shot noise ratio (SNR), methods of reusing the capacitor, such as an asynchronous reset [2], incremental sigma-delta modulators [3], [4], sigma-delta modulators [5], [6], and extended counting ADCs [7], [8], have been suggested. To enhance the DR more power efficiently without necessarily increasing the SNR, methods of varying the I-to-V conversion gain adaptive to the detector current have been introduced. The variable I-to-V gain has been implemented either by scaling the detector current, as is the case in parallel current mirroring [9], [10], or by controlling the integration time, as is the case in the use of an overflow gate [11], a

synchronous reset [12], [13], a non-destructive multiple readout [14], [15], [16], [17], and an autonomous electronic shutter [18], [19].

To enhance the frame rate by increasing the throughput of the analog readout, efforts have been made to integrate ADCs with the FPAs. As a result, the number of the ADCs used for the FPAs varies from one to as many as the number of pixels: a single off-chip ADC, a single on-chip ADC, per-column ADCs [7], [20], per-block ADCs [21], and finally per-pixel ADCs [2]-[6], [8], [16], [17]. The per-pixel ADC architecture appears to be most promising to overcome the limitations of the current IR FPAs because the per-pixel implementation not only maximizes the number of parallel converters that can be used to achieve a high frame rate, but also enables the pixel-level dynamic range control required to obtain a high dynamic range. However, the previously reported per-pixel ADC architectures that use an asynchronous reset [2], incremental sigma-delta modulators [3], [4], sigma-delta modulators [5], [6], extended counting ADCs [8], and single-slope ADCs with multiple readout [16], [17] typically increased the frame rate by compromising the dynamic range, or vice versa.

The trade-off between the frame rate and the dynamic range can be relaxed by employing an I-to-V gain control scheme [9]-[13], [18], [19] in each pixel to construct a floating-point ADC, which enhances the DR without much increase in power consumption [22]. By utilizing three-dimensional integrated circuit (3-D IC) technology, in which multiple transistor layers are connected by means of vertical through-wafer vias [23], [24], [25], we can increase the area available for each pixel sufficiently to accommodate a per-pixel floating-point ADC.

In this research, a per-pixel, current-mode, floating-point, dual-slope ADC [26] designed for long-wavelength infrared (LWIR) FPAs using 3-D IC technology is proposed. The ADC provides a significant increase in both dynamic range and frame rate without a substantial increase in power consumption or area. The proposed architecture is based on a dual-slope ADC, for which the operation can be divided into the integration phase (sampling) and the discharge phase (quantization). The dual-slope ADC has several benefits compared with other potentially small ADC architectures [2]-[8], [16], [17], [20].

First, the dynamic range can easily be increased without sacrificing the frame rate by modifying the integration time. Second, mismatch among the ADCs in an array, which is one of the major causes of the fixed pattern noise (FPN), can be corrected using the integration capacitor of the dual-slope ADC.

To increase the dynamic range of the dual-slope architecture, the proposed design employs a high-speed sample-and-hold electronic shutter that automatically adjusts the integration time of the ADC according to the amount of detector current [18], [19]. Once the input is sampled onto the capacitor, the sampled value is held until the end of the integration phase and is then quantized during the discharge phase. Compared with previously reported floating-point topologies, in which binary-weighted current mirrors and multiple ADCs operate in parallel for a single detector [9], [10] or a per-pixel ADC captures capacitor voltages much more rapidly than the target frame rate [16], [17], the proposed approach saves power and area by sampling only once per frame using one ADC per pixel.

To improve uniformity among the ADCs in the array, the comparator offset in each converter is cancelled using its own integration capacitor, while gain error is corrected digitally. The proposed ADC architecture is easily scaled to larger array sizes and is well-suited to 3-D integration because the pixel signals are processed in each pixel and can be routed using the through-wafer vertical vias within each pixel.

A prototype 16 x 16 ADC array in a 0.18-μm CMOS technology achieves a 19-bit dynamic range and 8-bit mantissa resolution at 3000 fps, with a power consumption of only 7 μW/pixel. A second prototype 16 x 16 ADC array integrated in a 3-D 0.18-μm fully-depleted silicon-on-insulator (FDSOI) technology attains similar performance. Furthermore, each ADC partitioned into three layers successfully fits within a detector size of 50 x 50 μm^2 and demonstrates A/D conversion using 3-D IC technology.

1.2 Organization

The remainder of this dissertation is organized into seven chapters. Chapter 2 introduces the IR imaging and FPA architectures that are used for the IR imaging systems. Chapter 3

reviews the topologies for on-focal-plane A/D conversion and describes various dynamic range enhancement techniques for FPAs. Chapter 4 proposes a per-pixel, floating-point, dual-slope ADC architecture designed for high dynamic range and high frame rate LWIR FPAs. Chapter 5 describes the design of the constituent circuits of the ADC, while Chapter 6 presents the implementation details of the 2-D and 3-D prototypes that are fabricated in a single-poly, five-metal 0.18-μm CMOS technology and a 3-D single-poly three-metal 0.18-μm FDSOI, respectively. Chapter 7 describes the test setup and presents the measurement results for the dynamic range, frame rate, mantissa resolution, and the transfer characteristic of the prototype ADCs. Chapter 8 summarizes the key ideas of the proposed ADC architecture and suggests avenues for future research.

Chapter

2 *Infrared Imaging*

Since infrared (IR) imaging utilizes photons emitted from an object, rather than photons reflected by an object, as is the case in visible imaging, the quality of IR imaging primarily depends on the photon emission, whereas that of visible imaging relies on both the illumination source and the reflection. Therefore, IR imaging is widely used in scientific, medical, industrial, and military applications, in which reliable data collection is important, whereas visible imaging is typically used in consumer electronics applications. This chapter presents an overview of IR imaging systems, detectors, and focal plane array (FPA) technologies, which together have facilitated the proliferation of IR imaging.

Section 2.1 describes the radiation and detection models on which IR imaging is based. Section 2.2 reviews the different kinds of IR detectors used to convert the IR radiation into electronic signals. Section 2.3 describes IR FPAs comprised of IR detectors and readout electronics that capture electronic images from the IR radiation. Section 2.4 describes a state-of-the-art staring hybrid IR FPA and identifies its limitations. Section 2.5 summarizes the chapter.

2.1 Infrared Radiation and Detection

2.1.1 Infrared Spectrum

Since it was first discovered in the 1800's, infrared (IR) thermal radiation has been used to measure the temperature of objects [27], [28]. When the IR spectrum is detected in the earth's atmosphere, the absorption of IR radiation in the atmosphere influences the observ-

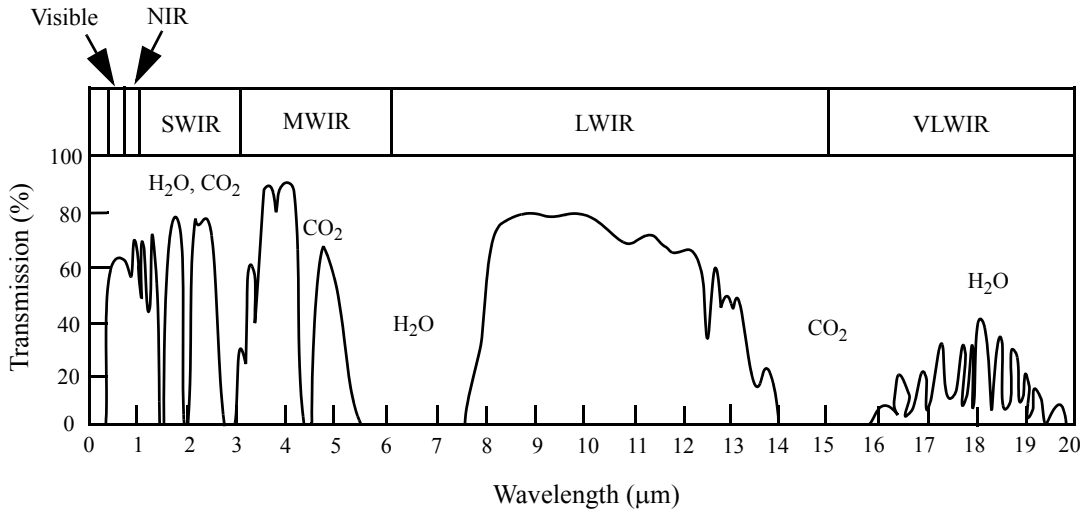


Figure 2.1: Typical transmission of the atmosphere.

able IR spectral range. Figure 2.1 shows a typical transmission in the earth's atmosphere, displaying several absorption peaks at which IR radiation is absorbed by CO_2 and H_2O in the atmosphere. The IR spectrum is divided into near IR (NIR; 0.7–1 μm), short-wavelength IR (SWIR; 1–3 μm), mid-wavelength IR (MWIR; 3–6 μm), long-wavelength IR (LWIR: 6–15 μm), and very long-wavelength IR (VLWIR: 15–20 μm) bands [27], [29].

2.1.2 Infrared Radiation

The radiant emittance from an object at wavelength λ and temperature T can be modeled by *Planck's law of black body radiation*

$$M(\lambda, T) = \frac{2\pi hc^2}{\lambda^5\left(\exp\left(\frac{hc}{\lambda kT}\right) - 1\right)}, \tag{2.1}$$

where h is the Planck's constant ($6.626\text{x}10^{-34}$ J·sec), c is the speed of light ($3\text{x}10^{8}$ m·sec^{-1}), and k is the Boltzmann's constant ($1.381\text{x}10^{-23}$ J·K^{-1}) [30]. The unit of the radiant emittance is W·cm^{-2}·sec^{-1}·μm^{-1}. By using the relationship between the radiant emittance and photon emittance of

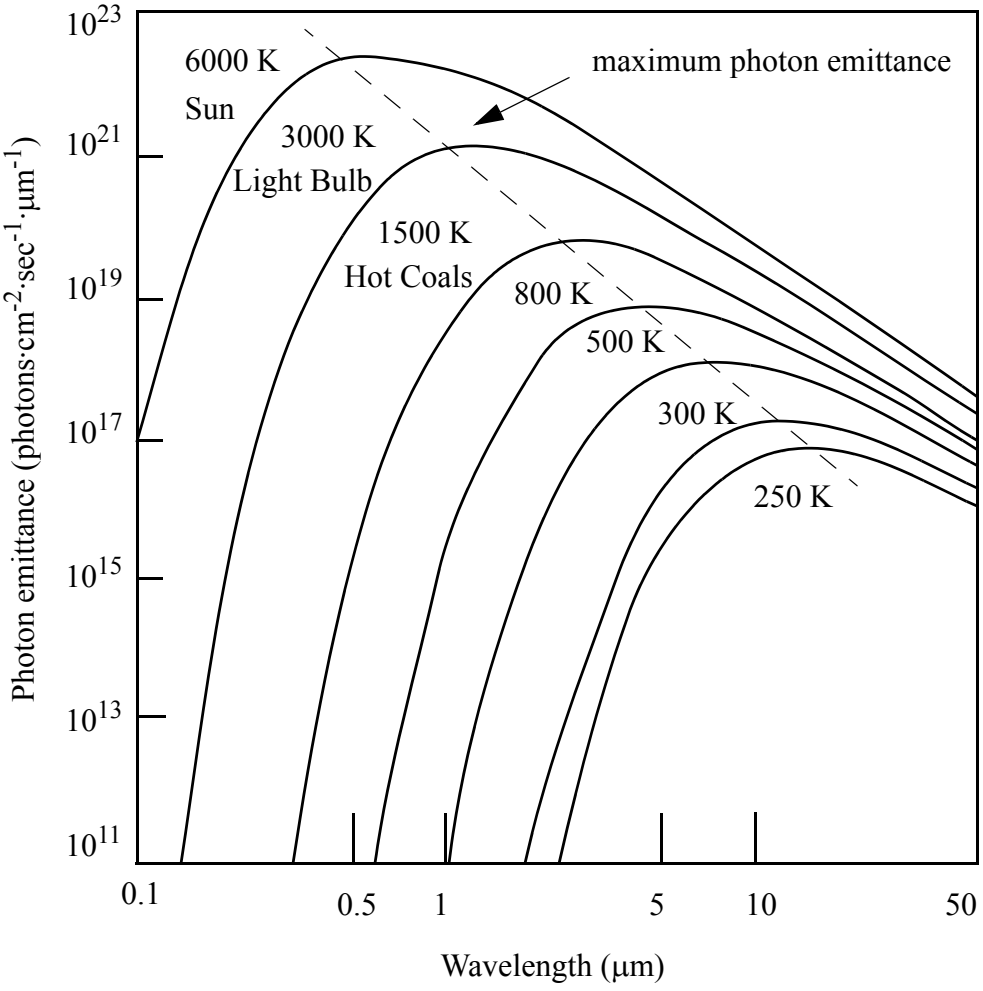


Figure 2.2: Photon emittance from a black body

$$M(\lambda, T) = \frac{hc}{\lambda} Q(\lambda, T) \quad , \tag{2.2}$$

the photon emittance can be written as

$$Q(\lambda, T) = \frac{2\pi c}{\lambda^4 \left(\exp\left(\frac{hc}{\lambda k T} \right) - 1 \right)} \quad . \tag{2.3}$$

The unit of photon emittance is photons·cm^{-2}·sec^{-1}·μm^{-1}.

Figure 2.2 plots the photon emittance of several objects with different temperatures. As shown by the dotted line, the wavelength of maximum photon emittance λ_m shifts to

smaller wavelengths as the object's temperature increases. This relationship is formulated by *Wein's displacement law*

$$\lambda_m T = a, \tag{2.4}$$

where a is 2897.8 μm·K for radiant emittance and 3669.7 μm·K for photon emittance [30].

In general, a better thermal resolution can be achieved using an IR spectrum band in which the radiant power peaks because the larger the incremental photocurrent is per temperature change, the easier it is to detect the change. For example, the temporal resolution can be increased by using the LWIR band for an object near room temperature, the MWIR band for a hot object of 800 K, and the visible band for the sun with a 6000-K surface temperature. However, the selection of the band utilized in various applications depends not only on the radiant peak, but also on practical constraints, such as the availability of the detectors and optical materials.

2.1.3 Infrared Detection

The IR power or photons emitted from an object can be collected by an IR detector and converted into proportional electrical signals. The output signal of an IR thermal detector is measured by integrating $M(\lambda, T)$ over the wavelength. Similarly, the output of a photon detector is obtained by integrating $Q(\lambda, T)$ over the wavelength. Since the IR photons pass through the earth's atmosphere and optics before they reach the IR detector, the total photocurrent i_{ph} collected by a detector of area A_d and quantum efficiency $\eta_d(\lambda)$ can be calculated as

$$i_{ph}(T) \approx \frac{qA_d}{4F^2} \int t_{atm}(\lambda) t_{opt}(\lambda) \eta_d(\lambda) Q(\lambda, T) d\lambda, \tag{2.5}$$

where q is electron charge of 1.602 x 10^{-19} C, F is f-number of the optics, $t_{atm}(\lambda)$ is the transmission of the atmosphere, and $t_{opt}(\lambda)$ is the transmission of optical materials [29].

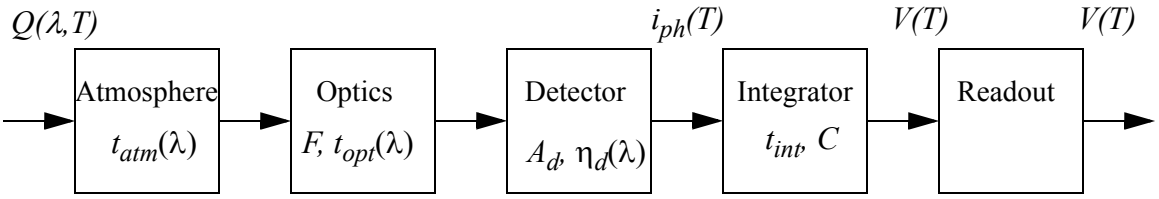


Figure 2.3: Block diagram of IR detection model.

The photocurrent is typically integrated onto an integrator of capacitance C for a certain integration time t_{int}, and the resulting voltage $V(T)$ sampled at the end of the integration is then

$$V(T) = \frac{i_{ph}(T)t_{int}}{C} . \tag{2.6}$$

The smaller the integration time, the faster the frame rate. The transformation of the signal in an IR photon detection model from the incident photon to the output voltage is summarized in Figure 2.3.

2.1.4 Background Limited IR Performance (BLIP)

When designing an IR imaging system, different sources of noise, such as photon shot noise, detector thermal noise, and readout circuit noise must be considered simultaneously to achieve an optimum performance. Unlike visible-wavelength imaging systems, IR imaging systems used in the atmosphere must detect small temperature differences in the range of 1 mK - 1 K in the presence of a large background radiation of 300-K room temperature, which is equivalent to detecting pA-range current differences in the presence of a nA-range current.

Due to the significant amount of the photocurrent generated by the background radiation, the performance of infrared imaging is fundamentally limited by the photon shot noise of the background when the power of all other noise sources is maintained below the

shot noise level. The performance of an IR imaging system limited only by the photon shot noise of the background radiation is referred to as the *background limited IR performance* (BLIP) [27].

Since photon shot noise is generated by the random arrival of incident photons (both background and signal photons) at the detector and described by a Poisson distribution [1], the signal-to-photon shot noise ratio (SNR) at the end of integration is proportional to the charge Q stored onto the integration capacitor. The SNR is given by

$$SNR = \frac{(i_{ph}t_{int})^2}{q i_{ph} t_{int}} = \frac{Q}{q} \leq \frac{Q_{max}}{q} , \tag{2.7}$$

where i_{ph} is the photocurrent, t_{int} is the integration time, q is the electron charge of 1.602 x 10^{-19} C, and Q_{max} is the maximum charge that can be stored onto the integration capacitor, usually referred to as the *charge-handling capacity.* The relationship of signal power, shot noise power, and the SNR to the integration time is illustrated in Figure 2.4.

The SNR in the BLIP operation is improved only by increasing the charge-handling capacity [1]. To achieve the maximum SNR at the increased capacity, the integrated charge at the end of the integration (i_{ph} x t_{int}) must be increased. Consequently, IR imag-

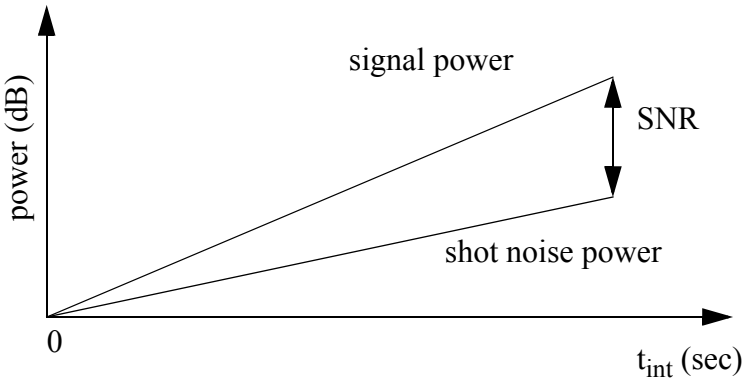


Figure 2.4: Relationship of signal-to-photon shot noise ratio to integration time.

ing systems typically employ both a large integration capacitance and a large detector in order to achieve a high SNR without sacrificing the frame rate.

2.1.5 Noise Equivalent Difference Temperature (NEDT)

One widely used measure for characterizing the performance of an IR imaging system, including the detector and the subsequent signal processing, is the *noise equivalent difference temperature* (NEDT). The NEDT is defined as the temperature change of a scene required to produce a detector signal equal to the rms noise of an IR imaging system [1]. A lower NEDT number means better thermal resolution. The NEDT is improved by reducing the noise contribution of the entire system. Therefore, to improve the NEDT, not only must the signal-to-photon shot noise ratio, as governed by the maximum integrated charge, be increased, but the detector thermal noise and readout circuit noise must also be reduced simultaneously.

2.2 Infrared Detectors

This section describes different types of IR detectors that convert IR radiation into electrical signals and defines several figures of merit used to describe the performance of the IR detectors. Depending on the conversion mechanism, IR detectors can be classified into thermal and photon detectors. In a thermal detector, the incident IR radiation changes the temperature of the detector, and as a result, the detector's electrical properties, such as resistance or capacitance. On the other hand, in a photon detector, an incident photon with energy greater than the bandgap of the detector directly excites the charge carriers in the material and generates measurable photocurrents. An excellent overview of IR detectors can be found in [27] and [28].

2.2.1 Thermal Detectors

Thermal detectors are usually operated at room temperature and are typically used in cost-sensitive commercial applications. Although the operation of thermal detectors is

conceptually very simple, they suffer from a trade-off between the sensitivity and the response time of the detection. To increase their sensitivity, detectors must be thermally isolated; however, to increase the response time, the built-up heat in the detector must be released quickly.

Among many different types of thermal detectors, thermocouples, pyroelectric detectors, and bolometers are the three most common [27]. A conventional thermocouple utilizes the thermoelectric effect to convert heat into a voltage difference. More advanced types of thermal detectors are pyroelectric detectors and microbolometers, which use a change in electrical properties, such as capacitance and resistance, respectively, to detect temperature changes. Pyroelectric detectors and microbolometers can be miniaturized to form two-dimensional (2-D) detector arrays.

2.2.1.1 Thermocouples

A thermocouple is constructed of two different metals that form two metallic junctions as shown in Figure 2.5. When different temperatures, T_0 and T_1, are applied to the two junctions, J_0 and J_1, respectively, a potential difference is measured between A and B. Seebeck discovered this effect in 1821 and demonstrated the first thermocouple [27]. To achieve a higher voltage, several thermocouples can be connected in a series, which is referred to as a thermopile.

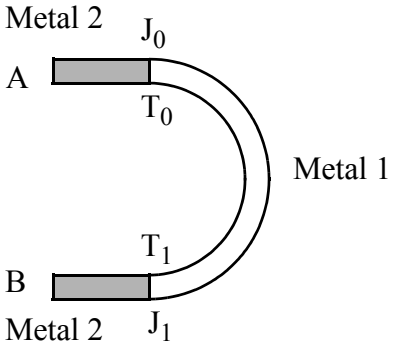


Figure 2.5: Thermocouple.

2.2.1.2 Pyroelectric Detectors

A pyroelectric detector changes its polarization when the temperature changes. This change in polarization can be detected if the rate of the change is faster than the rate at which the free charges in the detector redistribute and compensate for the change. We typically employ an optical modulator that chops the incident IR radiation to rapidly change the temperature of pyroelectric detectors. By reading the alternating current resulting from the change of polarization, we measure the temperature change [27].

2.2.1.3 Microbolometers

A microbolometer is composed of a temperature-sensitive resistive thin film suspended above the integrated readout electronics, as shown in Figure 2.6 [27]. The readout is composed of readout metal lines (x- and y-metals) and per-pixel transistor switches. The resistive thin film is called a thermistor, the resistance of which is changed when the temperature changes. Usually, vanadium oxide (VO_2) or amorphous silicon are used as thermistor materials. By applying a constant voltage across or a constant current through the thermistor, either a current change or a voltage change is detected. Much research effort has been devoted to developing new microbolometer materials and detection circuits to implement inexpensive IR detectors that operate at room temperature [27].

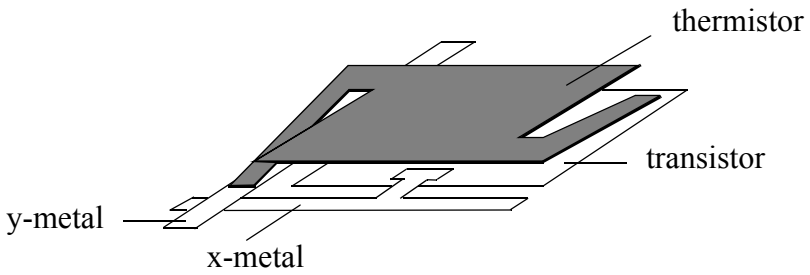


Figure 2.6: Microbolometer.

2.2.2 Photon Detectors

Although thermal detector technology has progressed enormously over the past decade, high-performance IR imaging applications still require photon detectors, which directly convert photons into charge carriers to achieve a high thermal resolution, a rapid response time, and good spectral selectivity [27]. Since most IR photon detectors are constructed using narrow-bandgap materials that can detect small-energy photons in the IR band, IR photon detectors are usually operated at cryogenic temperatures to reduce the detector thermal noise by suppressing the thermal generation of charge carriers in the detector materials [27].

Depending on whether an external electrical field is applied across the detector to read out electronic signals, photon detectors can be divided into photoconductive (PC) and photovoltaic (PV) detectors. As the incident photon flux increases, the conductivity of a PC detector increases, whereas in PV detectors there is an increase in photocurrent. As shown in Figure 2.7, a PC detector can be modeled as a variable resistance, R_{ph}, whereas a PV detector is modeled as a reverse-biased junction diode or a variable current source, i_{ph}, with an output impedance R_o.

Historically, PC detectors were developed first because the manufacturing process was simple [27]. They usually have a low output impedance and are used as a single detector or in a small array. Generally, the power consumption in PC detectors is large because an

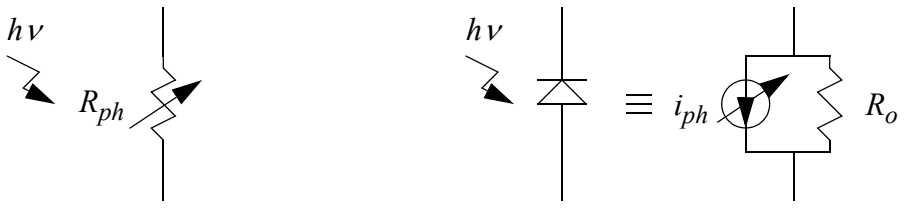


Figure 2.7: Models of (a) photocoductive detector and (b) phtovoltaic detector.

external electric field is required across the detectors to measure the change in conductivity.

PV detector materials were initially developed for 2-D staring FPAs, when charge coupled devices (CCDs) were invented in the late 1960's [31] and started to be used as a means of reading out the analog signal charges from 2-D arrays of detectors [32]. The high output impedance available in PV detectors helps to increase the injection of a detector current into the CCD multiplexers. The power consumption is small because PV detectors need only a small reverse bias across the p-n junction.

Depending on the optical excitation process, photon detectors can be classified into extrinsic, intrinsic, photoemissive, and quantum well detectors [27]. The corresponding band diagrams and example detector materials are shown in Figure 2.8 [33], [34].

2.2.2.1 Extrinsic PC Detectors

Extrinsic PC detectors depend on extrinsic absorption from the impurity level to the conduction band or from the valence band to the impurity level, as shown in Figure 2.8(a). Only majority carriers are created in the extrinsic absorption. Silicon (Si) and germanium (Ge) have been used as extrinsic PC detectors, and dopants such as Ga, As, Sn, and Hg are used to establish the impurity level. Although Ge was initially used because it was easier to grow pure Ge than Si, Si has become more popular due to the ease of integration with silicon readout electronics.

2.2.2.2 Intrinsic PC Detectors

Intrinsic PC detectors use intrinsic absorption from the valence band to the conduction band as shown in Figure 2.8(b). Unlike extrinsic absorption, the incident photons generate electron-hole pairs in intrinsic absorption. HgCdTe, PbS, and PbSe have been used to realize intrinsic PC detectors.

2.2.2.3 Intrinsic PV Detectors

As shown in Figure 2.8(c), the operation of an intrinsic PV detector is based on a p-n junction. Incident photons with energy greater than the bandgap of the detector material generate electron-hole pairs. Consequently, a current proportional to the incident photon flux is induced across the junction's potential barrier. The junction may be slightly reverse biased. Despite its difficult manufacturing process, the HgCdTe alloy system is one of the most popular intrinsic PV detectors due to its high quantum efficiency and the easy adjustment of its bandgap. The bandgap and, thus, the spectral response of the detector is adjusted by changing the composition ratio of CdTe with E_g = 1.6 eV and HgTe with E_g = 0 eV [1].

2.2.2.4 Silicide Schottky Barrier Detectors

A silicide Schottky barrier detector (SBD) uses photoemission over a Schottky barrier (0.21 eV - 0.23 eV), as shown in Figure 2.8(d). The silicide SBD is a type of PV detector and was discovered in 1973 [27]. Due to simpler fabrication and a faster response time than intrinsic PV detectors, the silicide SBD became popular for monolithic FPAs [27]. PtSi is the most popular material for realizing the silicide SBDs.

2.2.2.5 Quantum Well Infrared Photodetectors

Quantum well infrared photodetectors (QWIPs) use intersubband absorption within the conduction band or the valence band as shown in Figure 2.8(e), which allows the detection of IR radiation [1]. The QWIP is made using quantum wells of wide-bandgap materials, which individually do not absorb the IR radiation. Figure 2.8(e) illustrates a multiple quantum well structure formed by alternating thin layers (~50 Å) of GaAs and AlGaAs [33]. Although the bandgaps of GaAs and AlGaAs are too wide for IR absorption, the height of the quantum well is small enough to be used for IR detection. The width and the height of the quantum well are changed to adjust the spectral response of detectors (peak and cutoff wavelengths) [1].

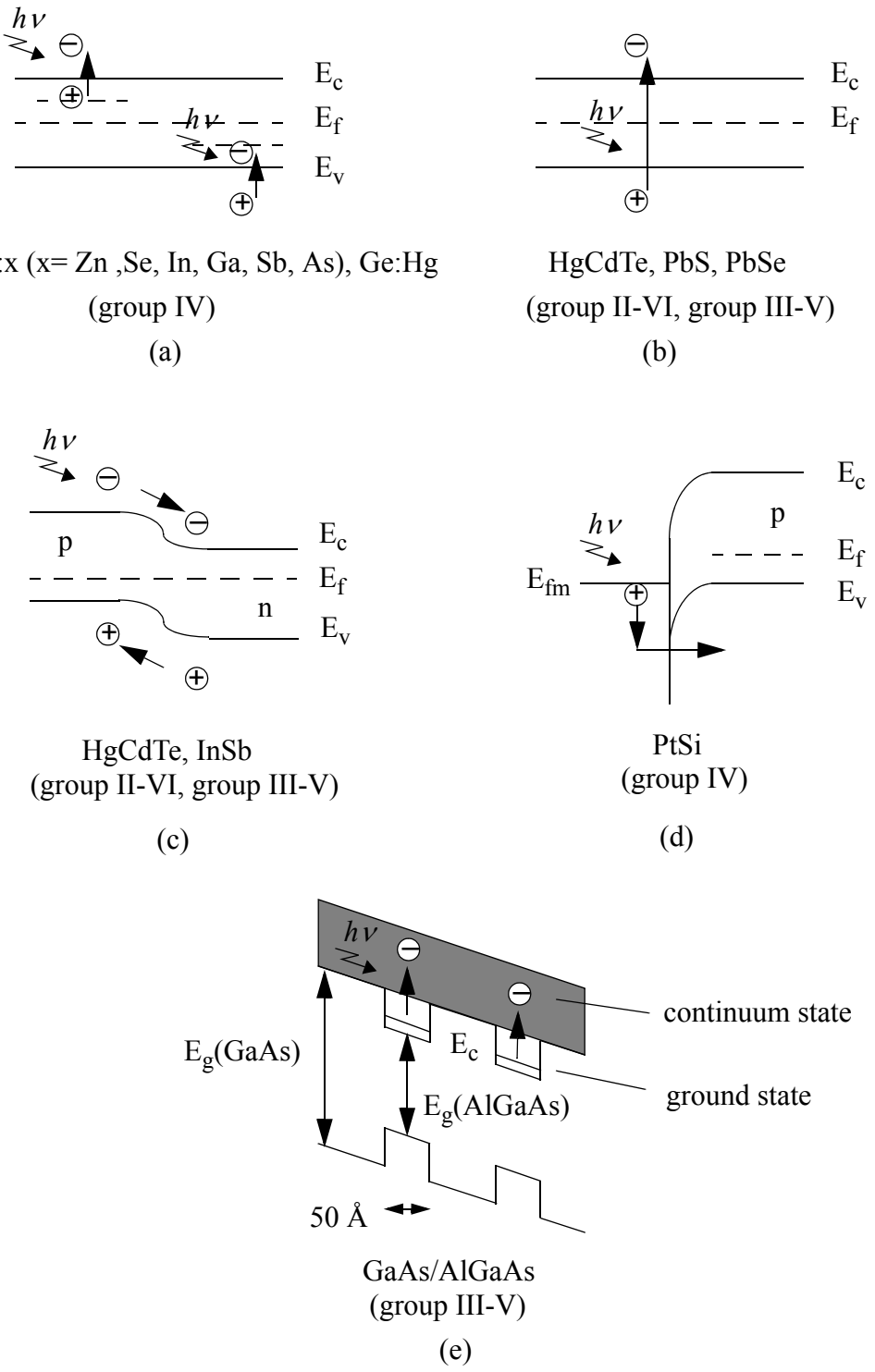


Figure 2.8: Band diagram of different IR photon detectors: (a) extrinsic PC detector, (b) intrinsic PC detector, (c) intrinsic PV detector, (d) silicide Schottky barrier detector, and (e) quantum well IR photodetector.

In the example of a GaAs/Al GaAs PC QWIP shown in Figure 2.8(e), intersubband absorption from the ground state within the quantum well to a continuum state is used. Once the carriers are excited by the IR radiation, the external electric field applied across the detector sweeps the excited carriers. The QWIP is emerging as an alternative to HgCdTe in both PC and PV detectors due to its high frequency selectivity, a high output impedance, and a higher temperature operation than HgCdTe detectors [1].

2.2.3 Detector Figures of Merit

Responsivity, noise equivalent power (NEP), and specific detectivity (D*) are commonly used to compare IR detectors. A more comprehensive list of metrics can be found in [30].

2.2.3.1 Responsivity

The responsivity of an IR detector is defined as the ratio of the rms output signal (voltage or current) to the incident power as

$$R_v = \frac{V_s}{\Phi}, \tag{2.8}$$

or

$$R_i = \frac{I_s}{\Phi}, \tag{2.9}$$

where Φ is the incident power, V_s is the rms signal voltage, and I_s is the rms signal current [27]. The units are V/W and A/W.

2.2.3.2 Noise Equivalent Power

Noise equivalent power (NEP) is defined as the amount of incident power required to produce a signal equal to the rms noise of a detector,

$$NEP = \Phi\frac{V_n}{V_s} = \Phi\frac{I_n}{I_s}, \tag{2.10}$$

where Φ is incident power, V_n is the rms noise voltage, V_s is the rms signal voltage, I_n is the rms noise voltage, and I_s is the rms signal voltage [27]. NEP is expressed in units of W.

2.2.3.3 Specific Detectivity

The specific detectivity, D*, is defined as

$$D^* = \frac{\sqrt{A_d \Delta f}}{NEP} , \tag{2.11}$$

where A_d is the detector area and Δf is the equivalent noise bandwidth [30]. The unit is $cm \cdot Hz^{1/2} \cdot W^{-1}$.

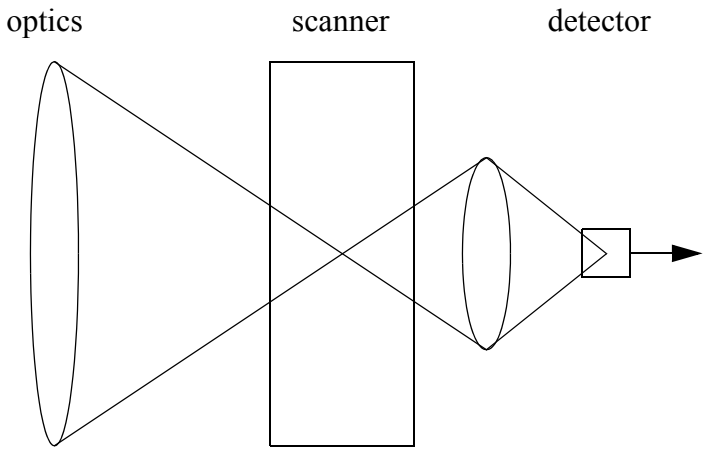
D* is the SNR of a detector with an area of 1 cm^2 and a bandwidth of 1 Hz when radiant energy of 1 W is incident on the detector. The higher the value of D*, the smaller signal the detector can detect. Shot noise from the background radiation sets a fundamental limit on D*. In practice, the thermal noise or the output resistance value of the detector can degrade D* by adding extra noise or by leaking photocurrent. When the output resistance of the detector is small, D* is degraded since the photocurrent of the detector leaks through the output resistor instead of being injected into the integrator.

2.3 Infrared Focal Plane Arrays

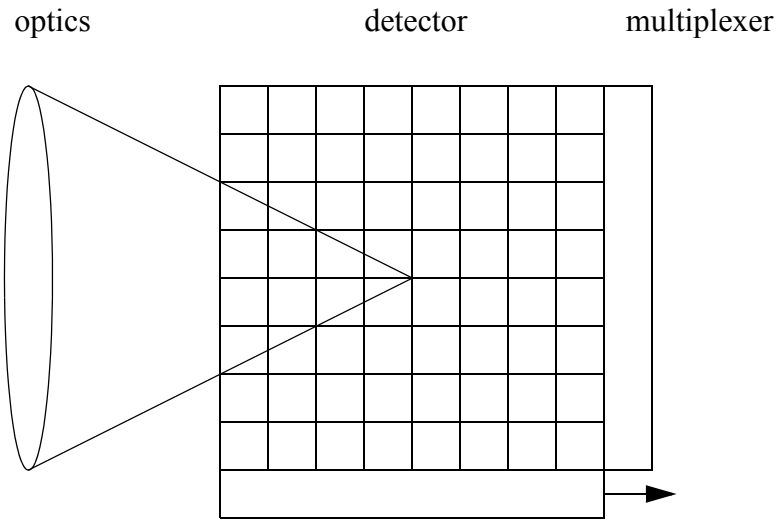
Since the 1950's, various FPAs and readout electronics have been proposed to capture two-dimensional (2-D) IR images [32]. As illustrated in Figure 2.9, there are two ways to capture 2-D images. The first method captures a 2-D image by scanning a scene with a single PC detector or a linear array of PC detectors, while the second stares at the scene with a 2-D detector array [33].

2.3.1 Scanning and Staring Arrays

In early years of IR imaging, a scanning FPA was the only means of capturing 2-D IR images. As shown in Figure 2.9(a), the scanning FPA is composed of optics, a single



(a)



(b)

Figure 2.9: (a) Scanning FPA and (b) staring FPA.

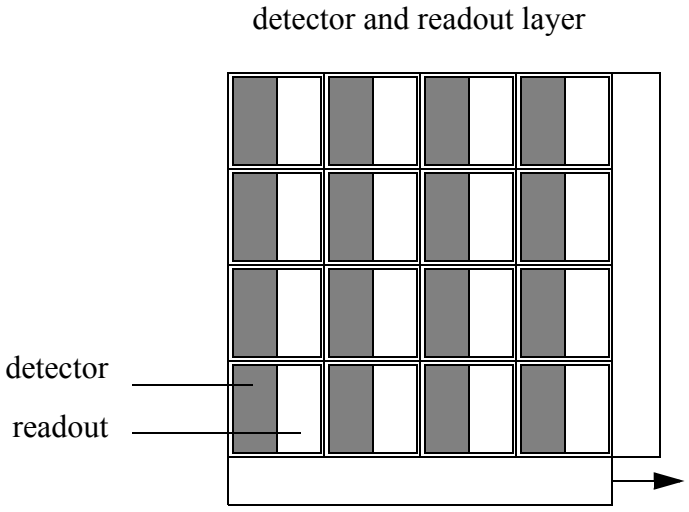
detector or a linear array of PC detectors, and a mechanical scanner that scans the entire focal plane.

The invention of the CCD and the development of PV detectors with a high output impedance made a staring FPA without a scanner possible [32]. As illustrated in Figure 2.9(b), the role of scanning mechanism was replaced by electronic multiplexers in staring FPAs, and the entire IR imaging system was simplified. Following the development of CCD multiplexers, other charge-transfer based multiplexers, such as a charge integration device (CID) and a charge injection matrix (CIM) were developed to reduce the large number of charge transfers in CCDs [34].

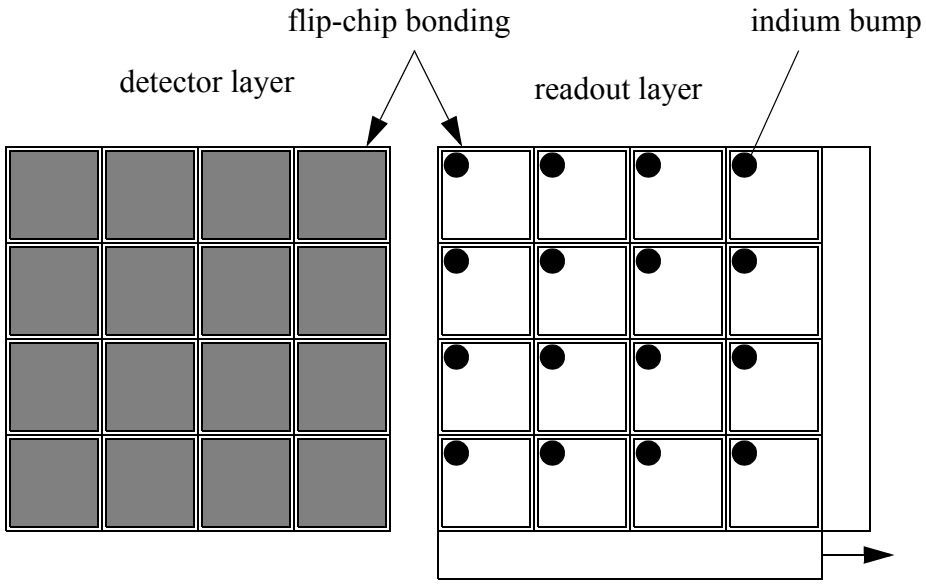
From the early 1990's, the improvements in CMOS technology have allowed low-noise multiplexing using CMOS circuits, and CMOS multiplexers have become dominant over previously developed charge-transfer based methods for analog multiplexing [1]. Unlike the charge-transfer based multiplexers, the signal in CMOS multiplexers is detected as a voltage rather than a charge. The CMOS readout circuitry in staring FPAs resembles that of digital memory.

2.3.2 Monolithic and Hybrid Arrays

Depending on the physical configuration of a detector array and the accompanying readout electronics, FPAs can be classified as monolithic and hybrid arrays. In a monolithic FPA such as that shown in Figure 2.10(a), both the detector array and silicon readout electronics (CCD or CMOS multiplexers) are fabricated in the same substrate. The monolithic integration of the detector array with the readout electronics is achieved either by using silicon detector materials, which can be fabricated with the silicon multiplexers in the same substrate, or by depositing non-silicon detector materials on top of the silicon multiplexers. Because of the constraints in manufacturing the detector array, the use of monolithic FPAs in IR imaging is limited to extrinsic silicon detectors, Schottky barrier detectors, or microbolometers. Monolithic FPAs are very popular in visible imaging



(a)



(b)

Figure 2.10: (a) Monolithic FPA and (b) hybrid FPA.

because the visible-range sensors typically made of silicon are easily integrated with multiplexers, A/D converters, and other digital circuits in CMOS technology [17].

If detectors are implemented in a fashion that is not compatible with silicon processing, a hybrid FPA shown in Figure 2.10(b) is used. The detector array and the readout electronics are fabricated on separate substrates using different materials, and a flip-chip bonding technology is used to combine the two layers [1], [35], [36]. Since the detectors and readout multiplexers are implemented on separate substrates, a fill factor of almost 100% can be achieved. In addition, the detector array and the readout electronics can be optimized separately to achieve improved performance for each layer. The alignment and thermal expansion match between the detector and the multiplexer layers have been improved to the level needed for commercial production over the past few decades. Hybrid FPA technology has been actively used in IR FPAs to combine the non-silicon IR detectors with the CMOS multiplexers, which are compatible with a cryogenic temperature operation. However, the integration of A/D conversion or other more complex circuits may require a better understanding of CMOS transistor performance at a cryogenic temperature, such as an increase in the threshold voltage [37], [38].

2.4 Staring Hybrid IR FPAs

Figure 2.11 illustrates a typical state-of-the-art staring hybrid IR FPA, usually operated at cryogenic temperatures to reduce the thermal noise of the detectors. Consequently, the total power consumption of detector array and the CMOS IC comprising the detector interface and readout electronics is constrained by the cooling consideration. In addition, the CMOS IC must fit within the same two-dimensional area as the detector array.

Figure 2.12 is a block diagram of the FPA. The detector interface electronics coupled to the detector array convert the detector current into a voltage by integrating the current onto an integration capacitor for a pre-determined integration time. The detector interface electronics must not only have low input impedance to improve the injection of the detector current into the interface electronics, but also stably bias the IR detectors to reduce the

detector current variation due to bias fluctuation. The sampled voltages from each pixel are usually read out through CMOS multiplexers and then fed to an external analog-to-digital converter (ADC). The signaling from the FPA to the ADC is typically single-ended.

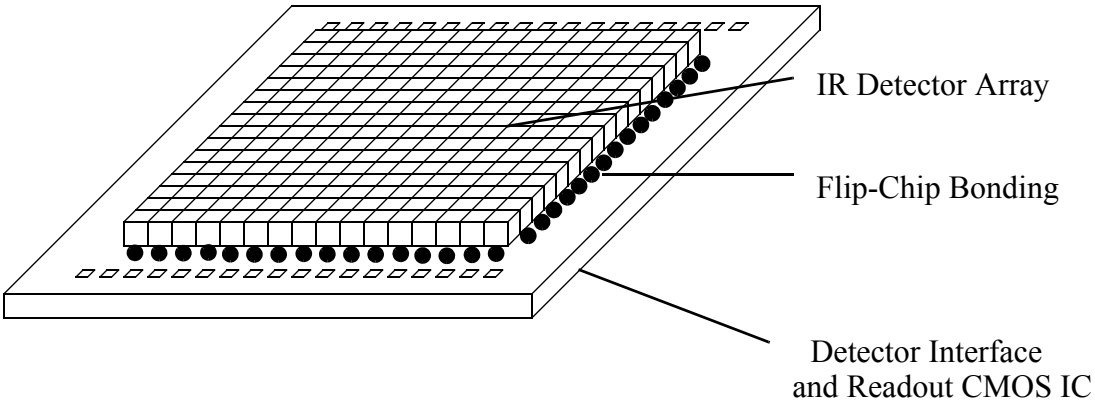


Figure 2.11: Staring hybrid IR FPA.

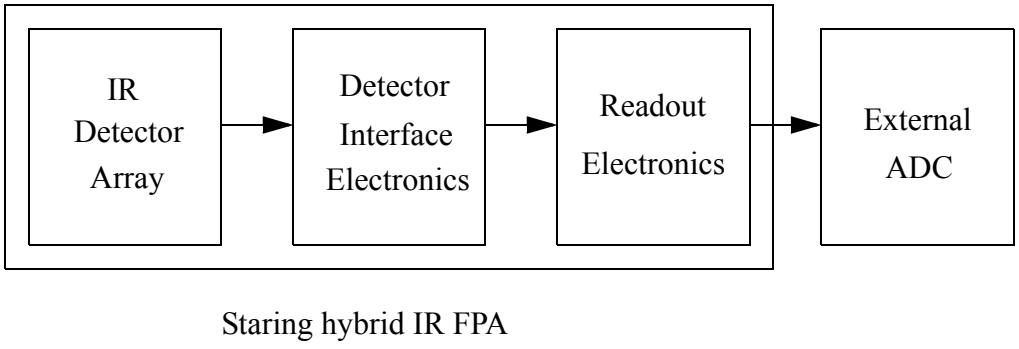


Figure 2.12: Block diagram of staring hybrid IR FPA.

2.4.1 Detector Array

Hybrid staring FPAs generally use PV, rather than PC, detectors because PV detectors consume less power. The detectors must have a large output resistance to ensure adequate injection of the detector current into the detector interface circuit. HgCdTe PV detectors are commonly used for staring hybrid FPAs [1].

2.4.2 Detector Interface Circuits

The efficiency with which detector current is injected onto the integration capacitor is determined not only by the output resistance of the IR detector, but also by the input impedance of the detector interface circuits. At the same time, the interface circuit has to provide stable biasing for the IR detector array to reduce a bias-related signal fluctuation, and it has to be small enough to fit within one pixel. Among many different approaches to implementing detector interface circuits [33], [39], [40], the four most commonly used methods are described: direct injection, buffered direct injection, a capacitive transimpedance amplifier, and gate modulation.

2.4.2.1 Direct Injection

Direct injection (DI) is one of the simplest ways to couple the IR detector to the integration capacitor. As shown in Figure 2.13(a), the detector current is injected onto the integration capacitor via a common-gate buffer. Since the input impedance of this buffer is the reciprocal of the g_m of the common-gate transistor, direct injection is widely used for large detector current applications, such as LWIR detection, in which the large background current flowing through the common-gate transistor helps to achieve a fairly large g_m. However, with this circuit it can be difficult to bias the IR detector for large dynamic range signals. Typically, the PV detectors are slightly reverse biased to maintain a low reverse leakage current in the detector [1] while preventing the detectors from being inadvertently forward biased. When the detector current changes significantly, so does the V_{GS} of the common-gate transistor. Consequently, the biasing of the detector can be disturbed.

In addition, a variation in the threshold voltage of the common-gate transistor can degrade the uniformity of the biasing in a 2-D detector array.

2.4.2.2 Buffered Direct Injection

To increase the injection efficiency of the direct injection method for small detector currents, negative feedback can be used to implement buffered direct injection (BDI), as shown in Figure 2.13(b) [41]. The input impedance of the BDI circuit is reduced by the gain of the feedback loop. In addition, this approach can accommodate a wide range of input currents, such as occurs in LWIR detection, without disturbing the biasing of the detector because the negative feedback helps to keep the input node voltage close to V_{b2} in Figure 2.13(b). The capacitance associated with flip-chip bonding shown in Figure 2.11 must be minimized because a large capacitance at the input node makes it difficult to stabilize the op-amp in the BDI circuit.

Compared with the capacitive transimpedance amplifier (CTIA) [33] approach explained below, the bias current of the op-amp can be much lower for large detector currents because the op-amp does not have to drive the large integration capacitor, but only the small gate capacitance of the common-gate transistor.

2.4.2.3 Capacitive Transimpedance Amplifier

In a CTIA, shown in Figure 2.13(c), the photocurrent is integrated onto a capacitor acting in feedback around a transimpedance amplifier. CTIAs enable the integration of extremely small detector currents by using a very small feedback capacitor. Therefore, they are not generally used for LWIR applications (in which large capacitance is required to suppress the photon shot noise from large background current), but are primarily used in MWIR, NIR, and visible applications. The detector biasing is very tightly regulated, as is the case in BDI. However, to handle a very wide detector current range, BDI can be implemented with less power dissipation than is the case for a CTIA.

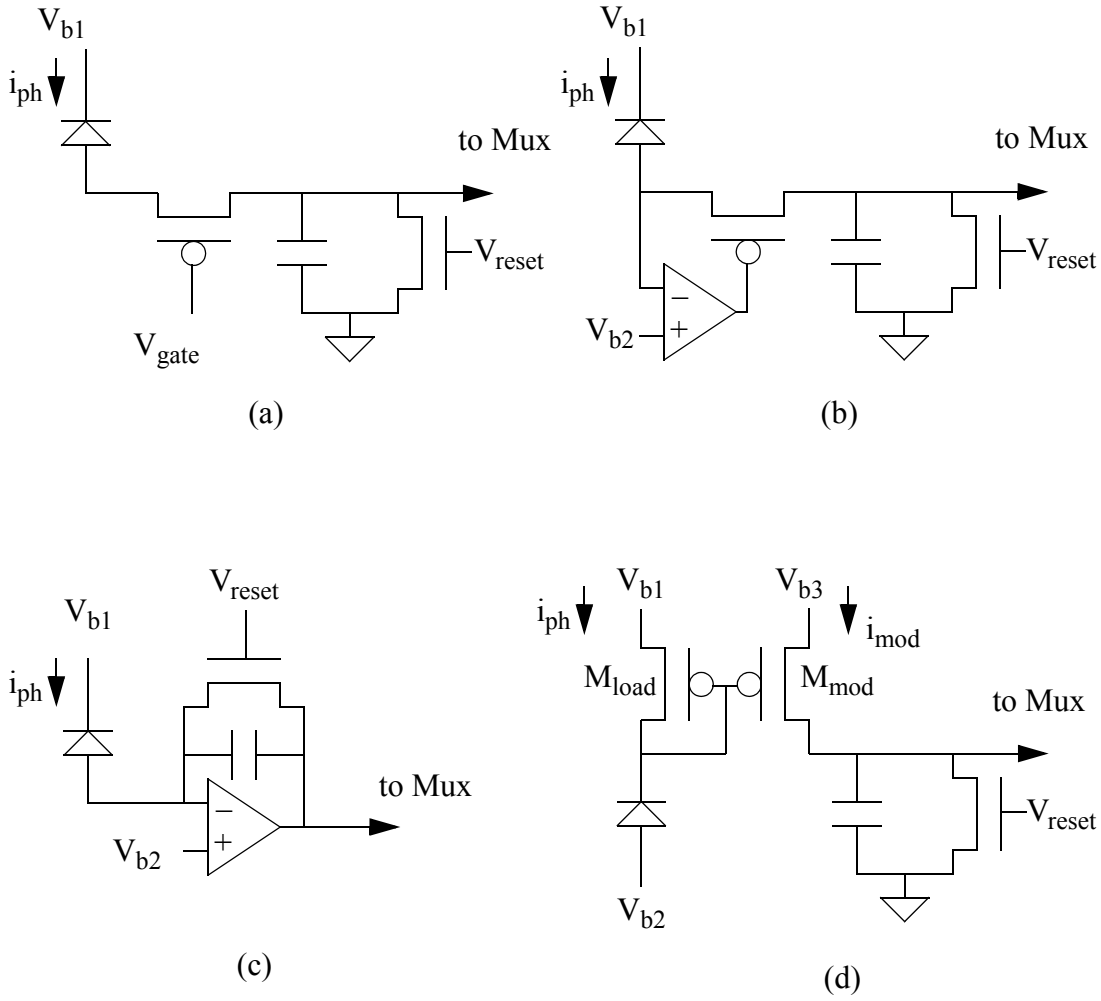


Figure 2.13: (a) Direct injection, (b) buffered direct injection, (c) capacitive transimpedance amplifier, and (d) gate modulation.

2.4.2.4 Gate Modulation

Unlike the interface circuits explained above, the gate modulation circuit shown in Figure 2.13(d) modulates the gate of the M_{mod} by using the load MOSFET M_{load} operating in weak inversion [42], [43]. By using the logarithmic relationship between the drain current and the gate voltage of the M_{load}, this structure automatically adjusts the current gain (i_{mod}/i_{ph}) of the current mirror. In addition, by varying V_{b3}, the dc current level of i_{mod} are

adjusted. Therefore, not only is a large dynamic range achieved, but also dc background current can be suppressed, which allows a smaller integration capacitor size. However, because M_{load} is operating in weak inversion, the variation of the threshold voltage of the M_{load} and changes of the V_{b1} bias significantly degrade the uniformity of the current gain across the FPA [43].

2.4.3 Readout Electronics and ADC

Once the detector current inputs are sampled onto the per-pixel integration capacitors, the sampled analog voltages are read out using an analog multiplexer. CMOS multiplexers dominate the analog multiplexing over CCD alternatives. A/D conversion is normally accomplished with an off-chip high-speed, high-resolution ADC.

2.4.4 Limitations of Staring Hybrid IR FPAs

Despite a very high thermal resolution, staring hybrid FPAs have not achieved very high frame rates together with a high dynamic range. When the integration time is small enough to allow a high frame rate, the frame rates of the FPAs are typically limited by the speed of the analog readout, not by the integration time, whereas the dynamic range is limited by saturation of the integration capacitors. To increase the frame rate and the dynamic range of a FPA within constrained area and power budgets, a simultaneous optimization of the detector interface circuit, the multiplexer, and the ADC is required.

2.5 Summary

This chapter presented IR focal plane imaging and reviewed IR detectors and FPAs. One of the most popular IR FPAs in high-performance applications employs a PV detector array integrated with a CMOS multiplexer and an external ADC. Even though this architecture can provide a high temperature resolution, its overall performance has been limited to relatively low frame rates and dynamic range due to the saturation of the integration capacitor and the limited throughput of the analog signal readout circuitry. In Chapter 3,

previous efforts to solve these problems are reviewed to provide a context for the subsequent discussion of the development of a high-frame rate, high-dynamic range IR FPA.

Chapter

3

High-Frame Rate, High-Dynamic Range Infrared Imaging

As mentioned in Chapter 2, the frame rate and dynamic range (DR) of state-of-the-art IR FPAs are typically limited by the analog readout circuits and saturation of the integration capacitor. Although various on-focal-plane ADC topologies and pixel-level DR enhancement techniques have been developed to improve the frame rate and the DR individually, it has been difficult to improve the frame rate and DR simultaneously due to the limited power budget and the small pixel area of the FPAs. Sections 3.1 and 3.2 review the previously reported techniques for enhancing the frame rate and DR, respectively. Section 3.3 describes a new FPA topology, called a *vertically-integrated sensor array* (VISA) [23], that increases the pixel area by stacking several transistor layers using a three-dimensional (3-D) integrated circuit (IC) technology [24], [25]. Section 3.4 presents a per-pixel floating-point dual-slope ADC architecture that achieves a high frame rate and a high DR simultaneously with low power consumption. Section 3.5 summarizes the chapter.

3.1 On-Focal-Plane A/D Conversion

In a sampled imaging system in which the photocurrent from a detector is integrated onto an integration capacitor for a specific integration time, after which the sampled capacitor voltage is read out, the frame rate of a FPA is typically limited by the analog readout from the detector array to the external ADCs. The readout speed can be improved by either

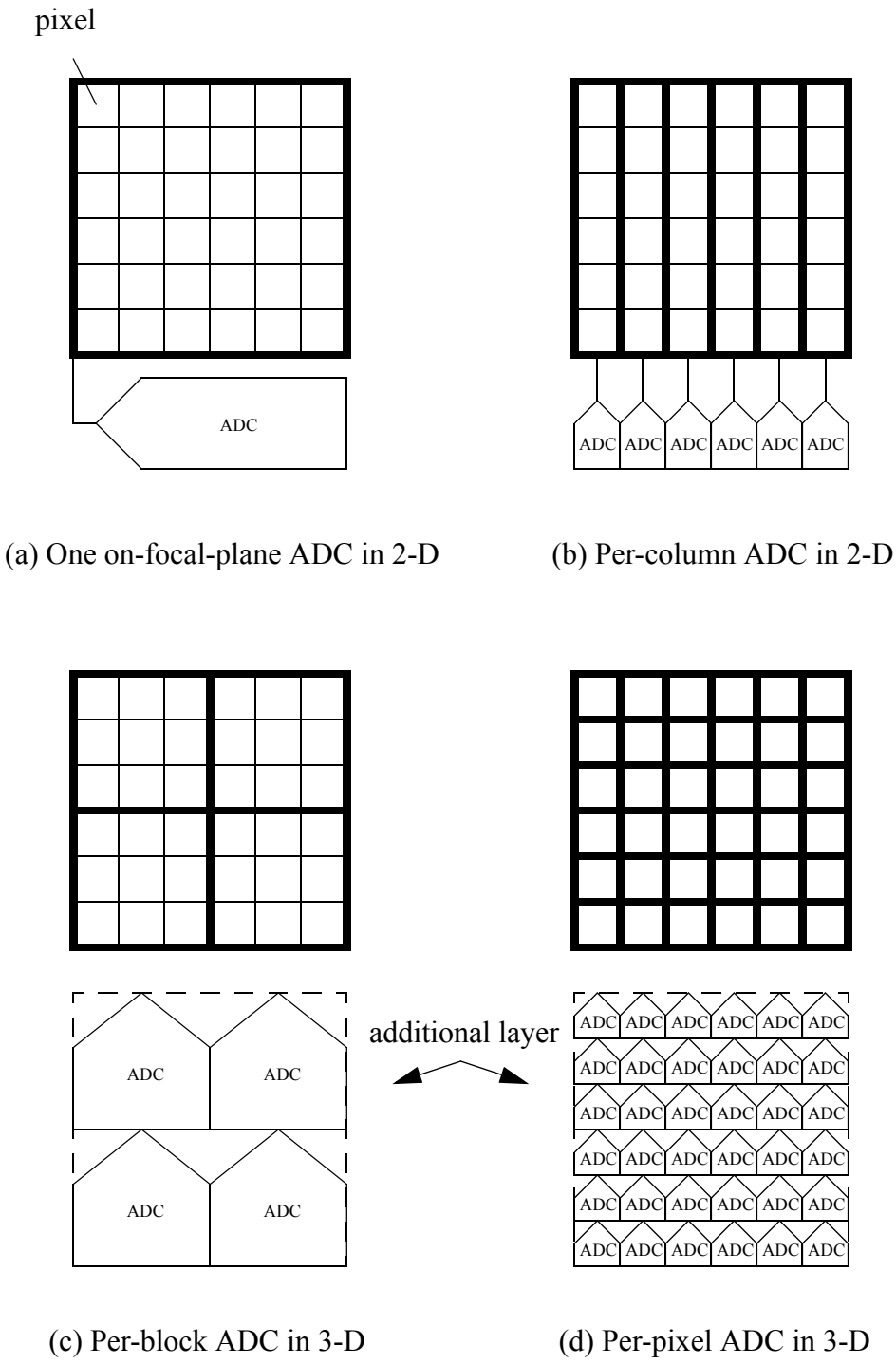
increasing the numbers of the analog readout channels and external ADCs or by integrating the A/D conversion into the FPA. Although the first approach can achieve a high frame rate, it typically results in considerably higher power dissipation than can be achieved with on-chip digitization.

Efforts to integrate data conversion circuits within FPAs first appeared in visible range imagers in which the detectors, the readout electronics, and the conversion circuits were all fabricated in a CMOS technology. The main motivation for these efforts was to achieve a monolithic CMOS camera that includes a detector array (silicon p-n junction diode), A/D conversion, and a digital signal processing. Later, similar efforts focussed on achieving a high-frame rate or a high-dynamic range IR FPAs [5], [7], [21].

Figure 3.1 shows various on-focal-plane ADC topologies realized in two-dimensional (2-D) and three-dimensional (3-D) integrated circuit (IC) technologies. The bold lines enclosing different numbers of pixels in the Figure indicate which pixels are processed by a single ADC. Figure 3.1(a) depicts a topology employing a single, high-speed ADC integrated with a FPA. This topology provides the bandwidth required for commercial video applications with frame rates of 30–60 fps. Several other approaches, such as per-column ADCs, per-block ADCs, and per-pixel ADCs, have been proposed to increase the number of parallel ADCs and, thus, the frame rates.

The per-column ADC architecture shown in Figure 3.1(b) can be used to increase the frame rate up to several hundred fps depending on the array size. Since the ADCs in this topology must be pitch-matched to the pixel width, it is difficult to employ large-size, high-performance ADCs. Moreover, this approach typically suffers from vertical fixed-pattern noise resulting from the mismatch among the per-column ADCs and amplifiers. Successive approximation ADCs and single-slope ADCs have been popular in this architecture [7], [20].

The per-block ADC approach illustrated in Figure 3.1(c) can be thought of as an evolution of the per-column ADC. By using the additional layers available in a 3-D IC technology, described in Section 3.3, the ADCs can be implemented in multiple layers



(a) One on-focal-plane ADC in 2-D

(b) Per-column ADC in 2-D

(c) Per-block ADC in 3-D

(d) Per-pixel ADC in 3-D

Figure 3.1: On-focal-plane ADC architectures in 2-D and 3-D IC technology.

underneath the detector layer. Relaxed from the area constraints of the per-column ADC topology, larger-area high-performance ADCs, such as pipeline ADCs, can be employed to further increase the frame rate [21]. The frame rate does not decrease as the array size increases because the number of the ADCs can be scaled proportionally. However, the complex analog routing from each detector to the input of the per-block ADC can limit the overall performance.

The per-pixel ADC topology shown in Figure 3.1(d) is a radical step toward fully parallel A/D conversion. Similar to the per-block ADC, this topology can achieve a high frame rate and easily scales to larger arrays without sacrificing the frame rate. The most difficult challenge of this topology is implementing the ADC within a small pixel area. Although very small ADC architectures, such as incremental sigma-delta modulators [3], [4], sigma-delta modulators [5], [6], and single-slope ADCs [16], [17], have been used for per-pixel A/D conversion, such implementations had to increase the pixel size to fit the ADC within the pixel. Fortunately, the area constraint can be relaxed by implementing the ADCs on the additional substrates available in a 3-D IC technology. Unlike the per-block ADC, the analog signal routing from the detector to the ADC can be simplified by using the vertical vias within each pixel.

3.2 Dynamic Range Enhancement Techniques

As explained in Chapter 2, a sampled imaging system converts a photocurrent i_{ph} into a proportional voltage V by integrating the current onto an integration capacitance, C, for an integration time, t_{int}. Then, the voltage is read out after the integration. The relationship of i_{ph} and V is

$$Q = CV = i_{ph} t_{int} . \tag{3.1}$$

The upper and lower bounds of the integrator output voltage range are determined by the saturation of the capacitor and by the noise level of the imaging system, respectively. The DR is defined as

$$DR = \frac{i_{max}}{\Delta i_{min}}, \tag{3.2}$$

where i_{max} is the maximum photocurrent that does not cause the integration capacitor to saturate, and Δi_{min} is the minimum detectable photocurrent difference, which is typically limited by the photon shot noise in the IR imaging system.

Although the DR can be increased by either decreasing Δi_{min} or increasing i_{max}, the latter method is favored in high-frame rate imaging because decreasing Δi_{min} typically requires averaging the output voltages over multiple frames, which reduces the effective frame rate. Therefore, to achieve a high frame rate and a high DR simultaneously, i_{max} must be increased by avoiding the saturation of the capacitor for large photocurrents.

According to Equation (3.1), there are three ways to avoid the saturation of the integration capacitor for large i_{ph}: increase the charge-handling capacity (defined in Chapter 2), decrease the integration current, or reduce t_{int}. The first method increases the charge-handling capacity of the integrator for large i_{ph} by subtracting a known amount of charge before it saturates. The second and the third methods reduce the i_{ph}-to-V conversion gain for large i_{ph} by scaling down i_{ph} and t_{int}, respectively. Since the first method increases the charge-handling capacity, it can improve both the DR and the SNR, whereas the second and the third methods increase only the DR by the maximum scaling ratios of i_{ph} and t_{int}, respectively. Typically, the second and third methods can be implemented with less power consumption than the first method. Moreover, they may be utilized as adaptive i_{ph}-to-V gain stages to construct floating-point ADCs in which the scaling ratio is the exponent of the floating-point ADC.

DR enhancement techniques can be applied on either a per-frame or a per-pixel basis. When the purpose of the imaging is to capture images that vary their brightness over time, a per-frame DR enhancement technique is used to increase the frame-to-frame DR. However, when the purpose is to capture images with both very bright and dark objects in the same frame, a per-pixel enhancement is used to enhance the intra-scene DR [44]. The following review focuses on the per-pixel DR enhancement techniques.

3.2.1 Scaling Charge-Handling Capacity

When the capacitance and voltage swing of the integrator are given, we can increase the charge-handling capacity of the integrator by subtracting a known amount of charge from the capacitor and recording the history of the subtraction *before* the integrator becomes full. Implementing this scheme requires both a comparator that monitors the voltage level of the integrator and a digital memory that records the history. To increase the charge-handling capacity, various methods have been proposed: simply counting the number of resets (an asynchronous reset scheme), subtracting charges synchronously to a clock (an incremental sigma-delta modulator and a sigma-delta modulator), and quantizing the residual capacitor voltage after the resets or the subtractions (extended counting).

3.2.1.1 Asynchronous Reset

Due to its simple structure, asynchronous reset has frequently been employed for pixel-level DR enhancement [2]. As shown in Figure 3.2, with this method the integration capacitor and counter are reset at the beginning of the frame, and the capacitor voltage, V_{cap}, is monitored using a continuous-time comparator. Each time the capacitor voltage reaches its maximum level V_{max}, the capacitor is asynchronously reset, and the counter records the total number of resets [2].

The minimum detectable photocurrent difference, Δi_{min}, of the asynchronous reset scheme is

$$\Delta i_{min} = \frac{CV_{max}}{t_{int}}, \tag{3.3}$$

where C is the capacitance of the integrator, and t_{int} is the integration time. i_{max} is simply Δi_{min} multiplied by the maximum number of asynchronous resets. Therefore, to achieve a high DR and a high frame rate simultaneously, the comparator must operate very fast. For example, to achieve a 20-bit dynamic range at 1 kfps, the comparator must operate at approximately 1 GHz (~ 2^{20} x 1000), which typically results in relatively large power dis-

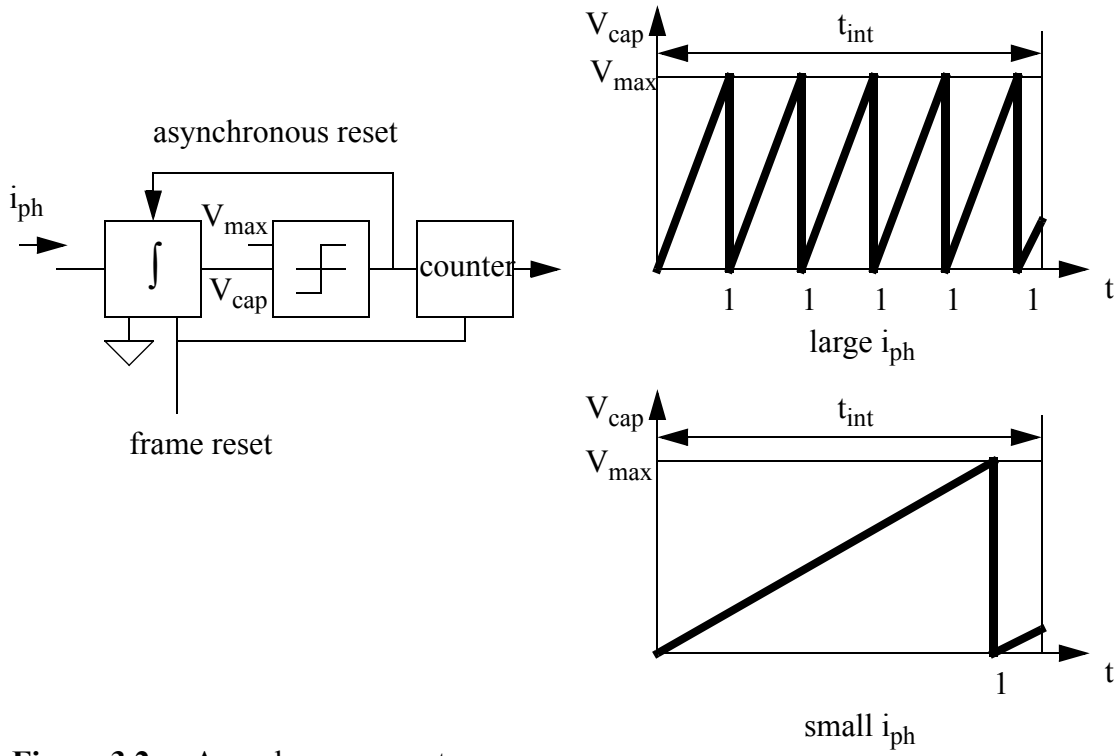


Figure 3.2: Asynchronous reset.

sipation. In addition, the comparator must have the same threshold level for fast-slope and slow-slope signals.

Because the Δi_{min} is not limited by the shot noise, but rather by V_{max}, in the asynchronous reset method, the DR can be increased by quantizing V_{max} rather than increasing the number of integrator resets. The incremental sigma-delta modulators and extended counting ADCs described below use two different approaches to quantizing V_{max}.

3.2.1.2 Incremental Sigma-Delta Modulator

As illustrated in Figure 3.3, the minimum detectable photocurrent difference, Δi_{min}, of the asynchronous reset scheme can be reduced by replacing the asynchronous reset with the subtraction of a fixed amount of charge from the integrator in a way that is synchronized to a clock *before* the integrator saturates. The subtraction history is stored in digital form. This scheme is typically referred to as *incremental sigma-delta modulation* and can be realized by either using a clocked comparator and a 1-bit digital-to-analog converter

(DAC) [3] or by simply re-timing the digital output of the asynchronous reset scheme [4]. To avoid the saturation of the capacitor, the former method needs twice the capacitance of the latter method.

Unlike conventional sigma-delta modulation, the integrator in an incremental sigma-delta modulator is reset at the beginning of every frame, and the output digital codes are completely determined by the input photocurrent levels. The input of the incremental sigma-delta modulator is restricted to DC or slowly varying signals. Figure 3.4 illustrates an example of the encoding of the different input photocurrent levels with an incremental sigma-delta modulator. The voltage waveforms of the integrator are shown in bold lines, and the encoded digital output bit streams are presented beneath the corresponding input photocurrents. An incremental sigma-delta modulator reduces the quantization step size by establishing more quantization levels (i_{ph}=2/3 and 1/3 in this example) in addition to the levels of the asynchronous reset scheme (i_{ph}=4/4, 3/4, 2/4, 1/4, and 0/4 in this example).

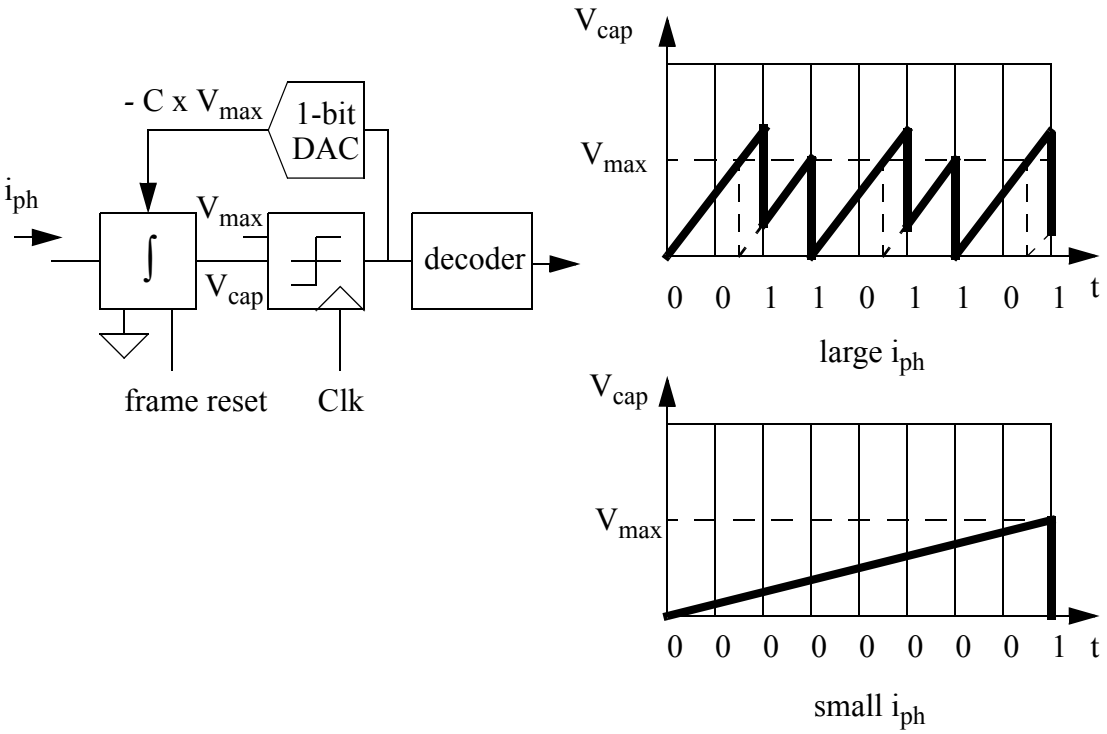


Figure 3.3: Incremental sigma-delta modulator.

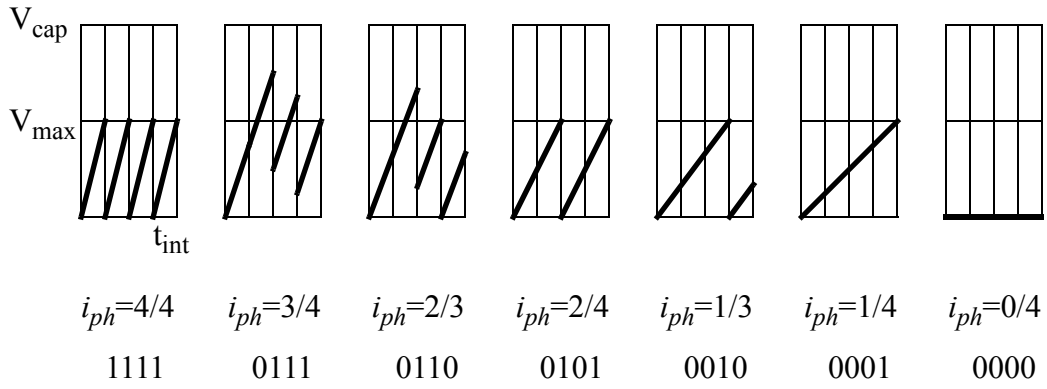


Figure 3.4: Encoding of incremental sigma-delta modulator.

3.2.1.3 Sigma-Delta Modulator

Conventional sigma-delta modulators without the frame reset have also been used for per-pixel ADCs to increase the DR by reducing the in-band quantization noise [5], [6]. In contrast to the incremental sigma-delta modulator, the input to a per-pixel sigma-delta modulator can be an AC signal whose bandwidth is determined by the time variation of the photocurrents. Similar to the incremental sigma-delta modulator, the need for accurate charge subtraction and digital filtering increases the area and power dissipation.

Compared to the asynchronous reset scheme, the power consumption of the comparator in both the incremental sigma-delta modulator and the sigma-delta modulator can be smaller because the comparators in these schemes operate more slowly to achieve a similar quantization step size. However, the overall attractiveness of these schemes for low-power per-pixel DR enhancement is not clear because the need for accurate charge subtraction in the feedback integrator can result in an increase in power consumption. In addition, the decoder needed for an incremental sigma-delta modulator and the digital filter for a sigma-delta modulator require additional area and power.

3.2.1.4 Extended Counting ADC

In an extended counting ADC, the quantization step size is reduced by quantizing the residual capacitor voltage using a multi-bit ADC, as shown in Figure 3.5. Therefore, the DR can be increased without employing the very fast comparator required in the asynchronous reset scheme. For example, a 20-bit DR at 1 kfps can be achieved using an 8-bit ADC and a comparator clocked at 4 MHz (~2^{12} x 1000), compared to the 1-GHz comparator without the ADC needed in the asynchronous reset approach.

The first reported implementation of an extended counting ADC in CMOS employed an incremental sigma-delta modulator and a multi-bit ADC [7]. The operation of this implementation is similar to that of the incremental sigma-delta modulator, except that the residual capacitor voltage at the end of the frame is quantized using a multi-bit ADC. This implementation is very similar to a sigma-delta modulator that is comprised of a multi-bit ADC and a single-bit feedback [45]. Since the counting operation could, instead, be

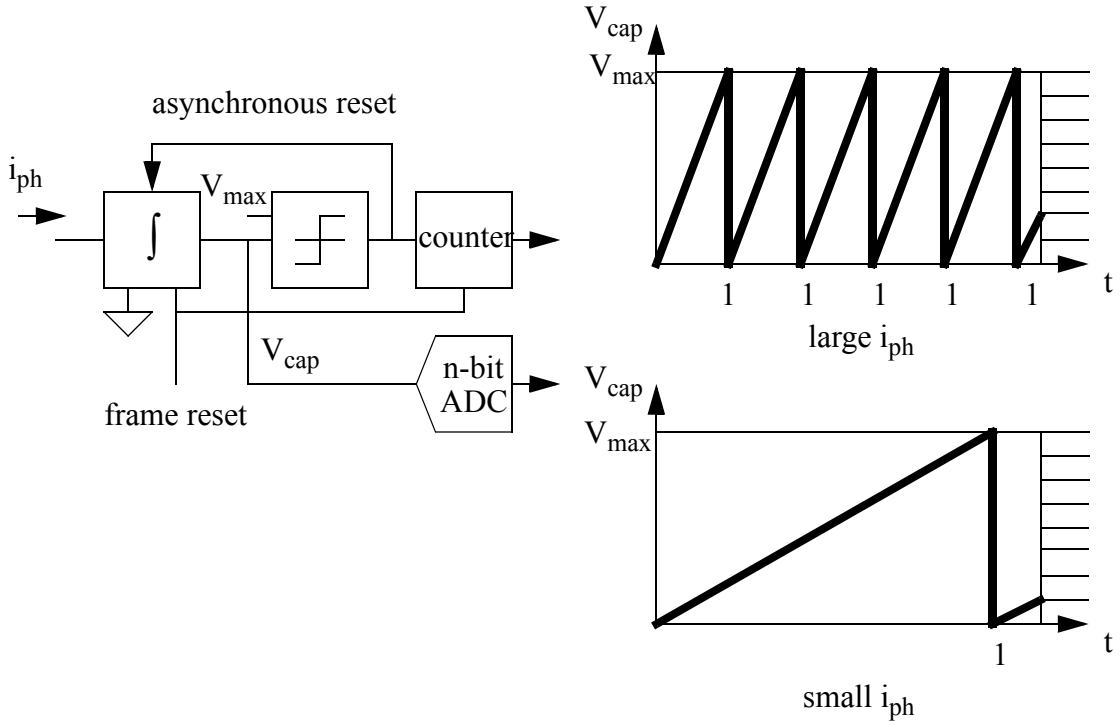


Figure 3.5: Extended counting using incremental sigma-delta modulator.

implemented using asynchronous reset, another implementation using asynchronous reset and a multi-bit ADC has been proposed to implement the extended counting ADC, as shown in Figure 3.5 [8].

The DR enhancement techniques explained thus far rely on the subtraction of charge from the integration capacitor to increase its charge-handling capacity. Consequently, although these schemes can increase the DR and the SNR simultaneously, they suffer from a trade-off between the DR and the frame rate. For those applications in which only a large DR range is required, a floating-point ADC can be used to relax the trade-off between the DR and the frame rate. To implement the variable i_{ph}-to-V gain stage required in a floating-point ADC, either the photocurrent or the integration time can be scaled. Section 3.2.2 describes a method of scaling the photocurrent, and Section 3.2.3 explains a method of scaling the integration time.

3.2.2 Scaling Photocurrent

When the circuit area and power consumption for each pixel are not constrained, as is the case in a high energy particle detection module, the trade-off between the DR and the frame rate can be relaxed using parallel integrators, as shown in Figure 3.6 [9], [10]. The input photocurrent is split into binary weighted currents, and those scaled currents are integrated onto parallel integrators to be converted into voltages. Among the integration capacitor voltages, the largest unsaturated voltage is selected as the mantissa value, and the inverse of the current scaling factor of the selected branch becomes the exponent value. For the example shown in Figure 3.6, a scaling factor of 1/8 is selected for a large photocurrent, and a scaling factor of 1 is selected for a small photocurrent. Although its large size and power consumption prohibit the use of this architecture in the IR FPAs, this method suggests a way of achieving a high DR and a high frame rate simultaneously by eliminating the fast resets or the charge subtractions required in the capacitor reuse methods.

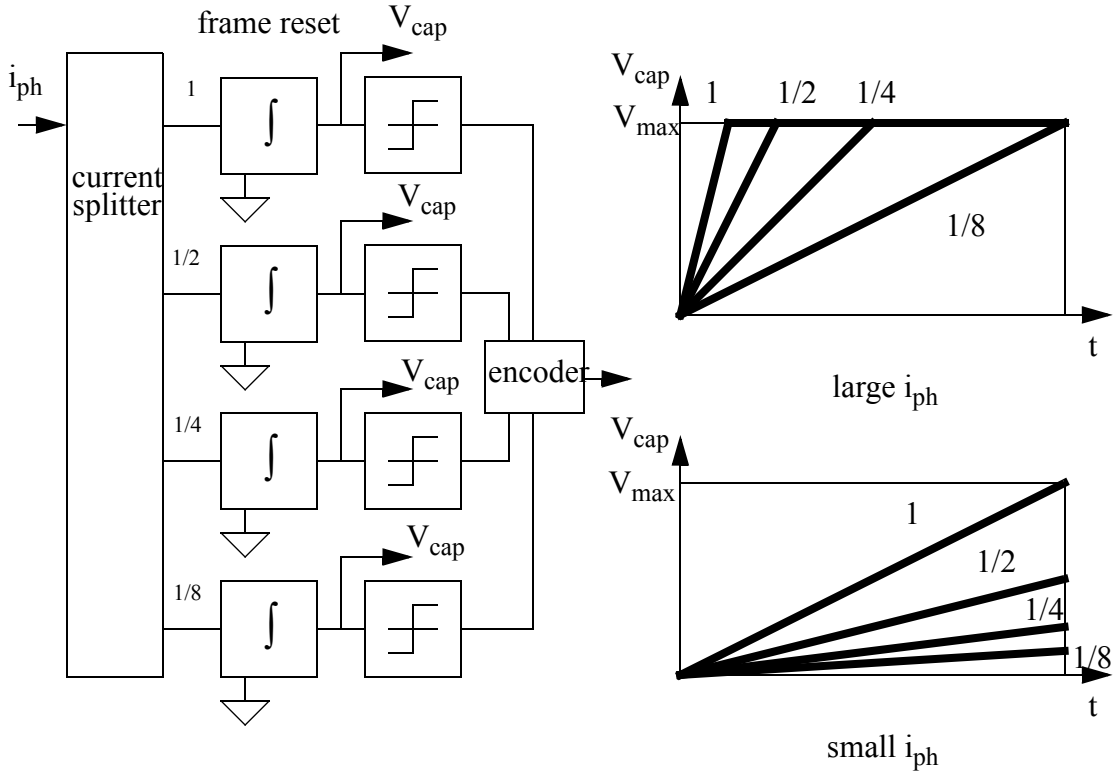


Figure 3.6: Binary-weighted current splitter.

3.2.3 Scaling Integration Time

The trade-off between the DR and frame rate can be relaxed without much increase in power consumption and area by using shorter integration times for larger photocurrents in order to prevent saturation of the integration capacitor. Since the longest integration time determines the frame rate, the use of shorter integration times does not reduce the frame rate. To select the shorter or longer integration times based on the signal strength, various integration time control methods have been suggested.

One method of adjusting the integration time is to change the gate voltage of a reset transistor that is connected to the integrator. A second method uses synchronous resets to achieve the same goal. A third method reads the voltage of the integration capacitor multiple times to select the optimum integration time. A fourth method varies the integration

time according to the signal strength by using a voltage comparator and an electronic shutter. Excluding the multiple readout method, the integration times automatically adapt to the strength of the photocurrents.

3.2.3.1 Overflow Gate

By changing the gate voltage of the reset transistor shown in Figure 3.7, which is referred to as a lateral overflow gate in this scheme, the optimum integration time can be selected automatically for large and small photocurrents [11]. The gate voltage controls the threshold voltage of the integrator, above which the integrator leaks charge through the overflow gate. The lower the gate voltage, the higher the threshold voltage, which is shown by dotted lines in Figure 3.7. The small photocurrent does not leak through the overflow gate because the threshold voltage increases at a rate faster than the actual integrator voltage, whereas the large photocurrent leaks through the overflow gate after the integrator voltage

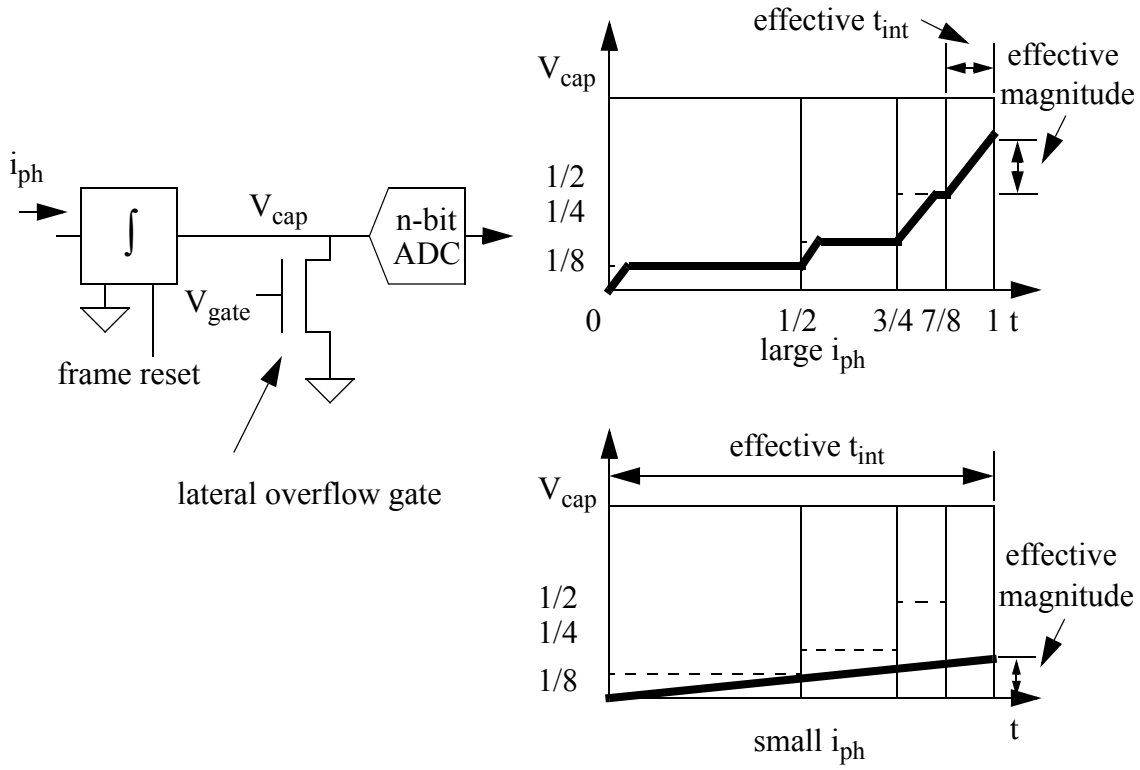


Figure 3.7: Integration time control using overflow gate.

reaches the threshold voltage. Therefore, the effective integration time of the large photocurrent is smaller than that of the small photocurrent. The photocurrent is measured by using the effective integration time and the effective magnitude shown in Figure 3.7. Since the gate voltage must be adjusted over time to control the threshold voltage, the analog gate voltage must be carefully routed. In addition, the threshold voltage variation of the overflow gate transistor increases the fixed pattern noise, which typically requires additional correlated double sampling.

3.2.3.2 Synchronous Reset

The optimum integration time can be implemented using synchronous resets and multiple comparison levels, as illustrated in Figure 3.8 [12], [13]. In this method, the capacitor is reset at one of several possible synchronous reset times (1/2, 3/4, and 7/8 in this example) depending on when the capacitor voltage rises above the comparison level, V_{ref}, illus-

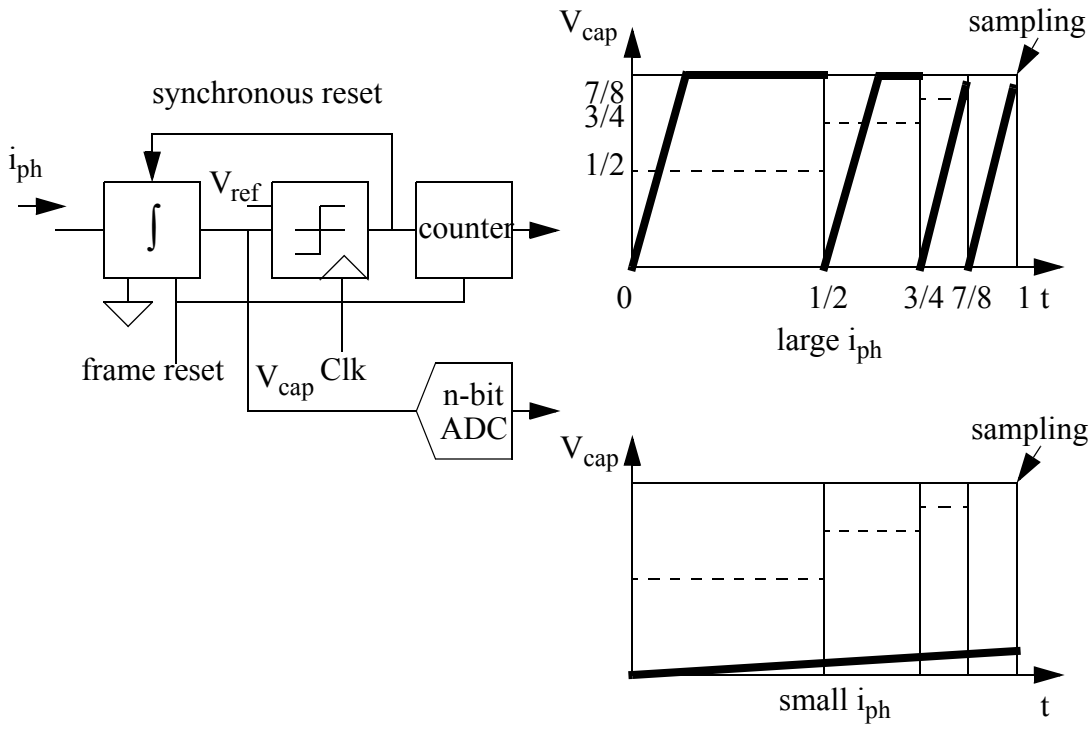


Figure 3.8: Integration time control using synchronous reset.

trated by the dotted line, and the integration starts over again from the reset voltage. Although the threshold voltage-dependent fixed-pattern noise is reduced by replacing the overflow gate with the reset switch, careful analog signal routing is still required because the reference level must still be adjusted over time.

3.2.3.3 Non-Destructive Multiple Readout

The idea of using non-destructive multiple readouts was first implemented in a dual sampling architecture that utilized two different integration times: short and long [14], [15]. Subsequently, the number of readouts was increased to further enhance the DR [16], [17]. The multiple readout method digitizes the integration capacitor voltage at many different integration times and stores the digital values in frame buffers as illustrated in Figure 3.9. Then, the maximum unsaturated capacitor voltage and the corresponding integration time are selected from the read out values.

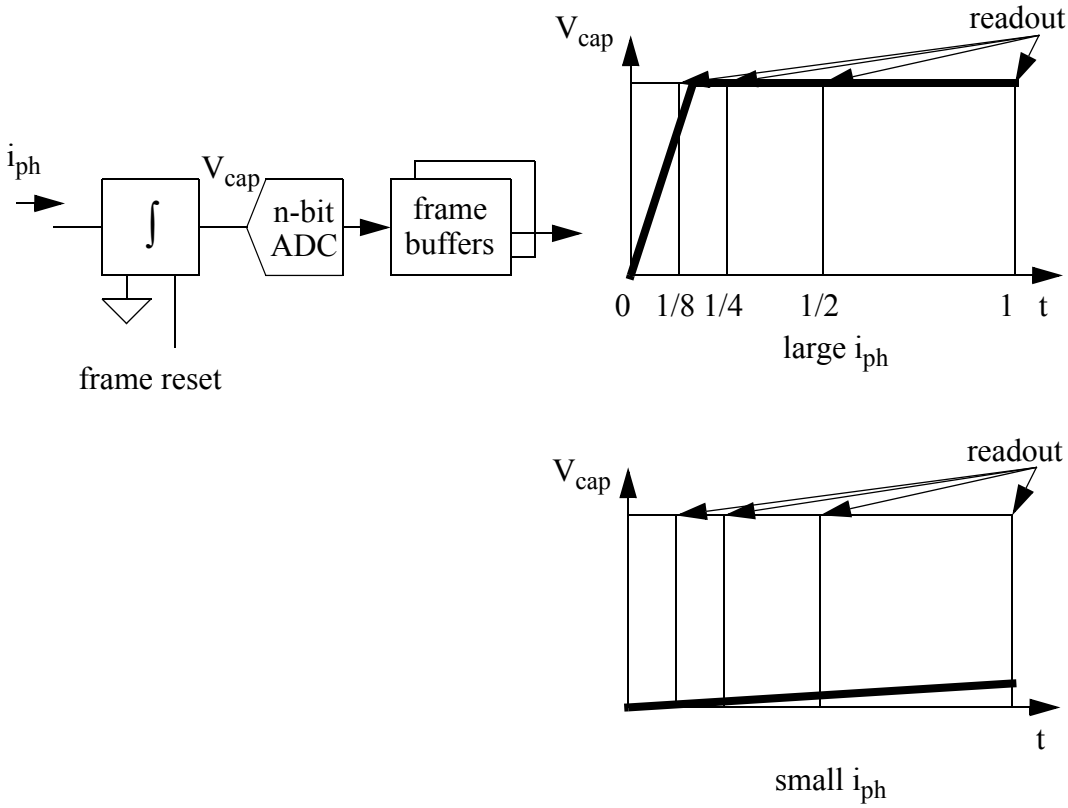


Figure 3.9: Integration time control using multiple readout.

The inverse of the integration time determines the relative strength of the signal. Therefore, a floating-point representation of the photocurrent is achieved using this method [16], [17]. The assignment of the mantissa and the exponent are similar to that of the parallel integration method using the binary-weighted current splitter explained in Section 3.2.2. The difference between these two methods is that the exponent is determined by the length of the integration time in the multiple readout method, rather than by the current scaling factor. Although this method increases the DR significantly, the conversion rate of the ADC must be much faster than the frame rate to digitize the multiple readouts, and extra frame buffers are required to store the digitized intermediate data.

3.2.3.4 Electronic Shutter

As illustrated in Figure 3.10, the integration time can be controlled using an electronic shutter and a comparator that monitors the capacitor voltage [18], [19]. After the frame

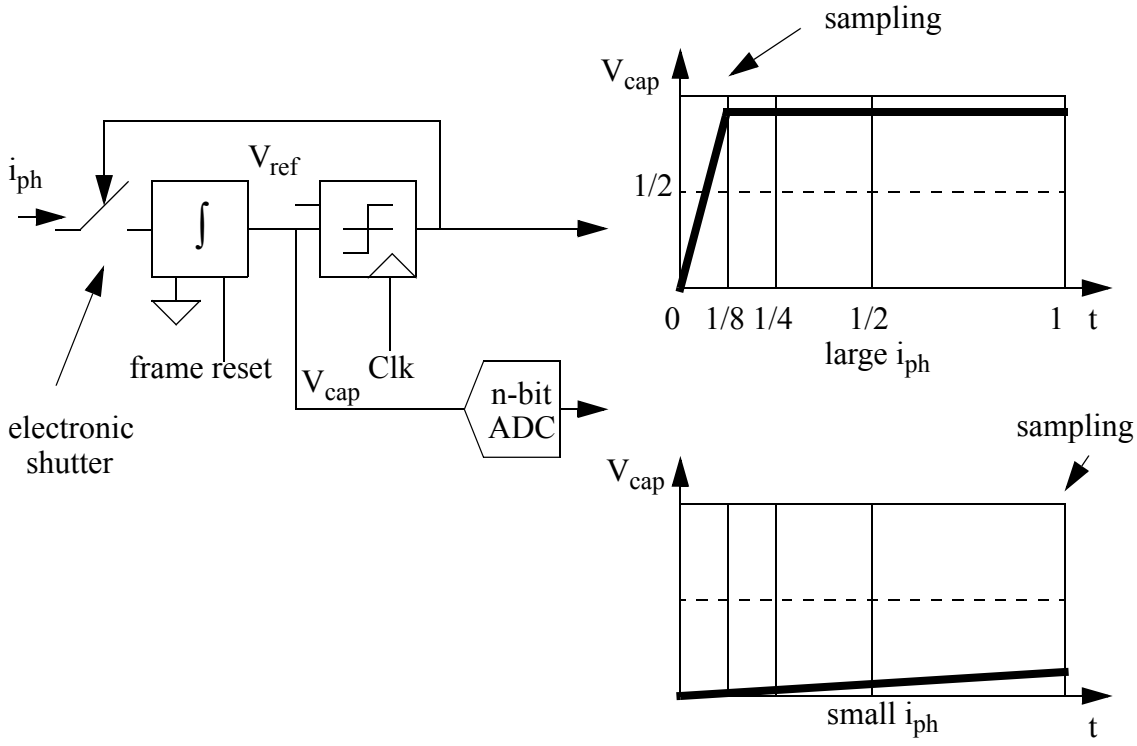


Figure 3.10: Integration time control using electronic shutter.

reset signal resets the integrator, the photocurrent is integrated onto the capacitor, and the capacitor voltage is compared with V_{ref} at each sampling point. Only when the capacitor voltage is higher than the reference voltage, is the capacitor sampled and the voltage held until the end of the integration. This method is similar to the synchronous reset method except that the synchronous reset method alters the beginning of the integration, whereas this method varies the end of the integration [18]. Because the beginning of the integration is fixed in this method, the reference voltage V_{ref} for the comparator can be fixed to $V_{max}/2$, which simplifies the generation of the reference voltage and its routing. By combining the electronic shutter with a uniform ADC, a low-power and area-efficient floating-point ADC can be implemented.

3.3 Vertically-Integrated Sensor Array (VISA)

As briefly mentioned in Section 3.1, a three-dimensional (3-D) IC technology can reduce the pixel size of the FPAs by implementing the readout electronics on multiple layers. A *vertically-integrated sensor array* (VISA) [23] is a new FPA architecture that combines a state-of-the-art hybrid FPA with a 3-D IC technology [24], [25]. As shown in Figure 3.11, the VISA replaces the conventional single-layer readout electronics with multiple layers that are connected by through-wafer vias. In contrast to the Z-technology of the 1980's, which used stacked IC layers placed perpendicularly to the 2-D detector array in order to increase the pixel area [46], the 3-D IC technology employed in the VISA uses through-wafer vertical vias to connect the transistors in multiple IC layers to increase the pixel area.

The VISA retains all the benefits of the hybrid FPA and provides increased circuit area. By using the increased circuit area, we can accommodate more advanced readout electronics to enhance the frame rate and DR simultaneously. Moreover, by optimizing the frame rate and DR enhancement blocks together, we can develop a new ADC architecture that minimizes both the area and the power consumption.

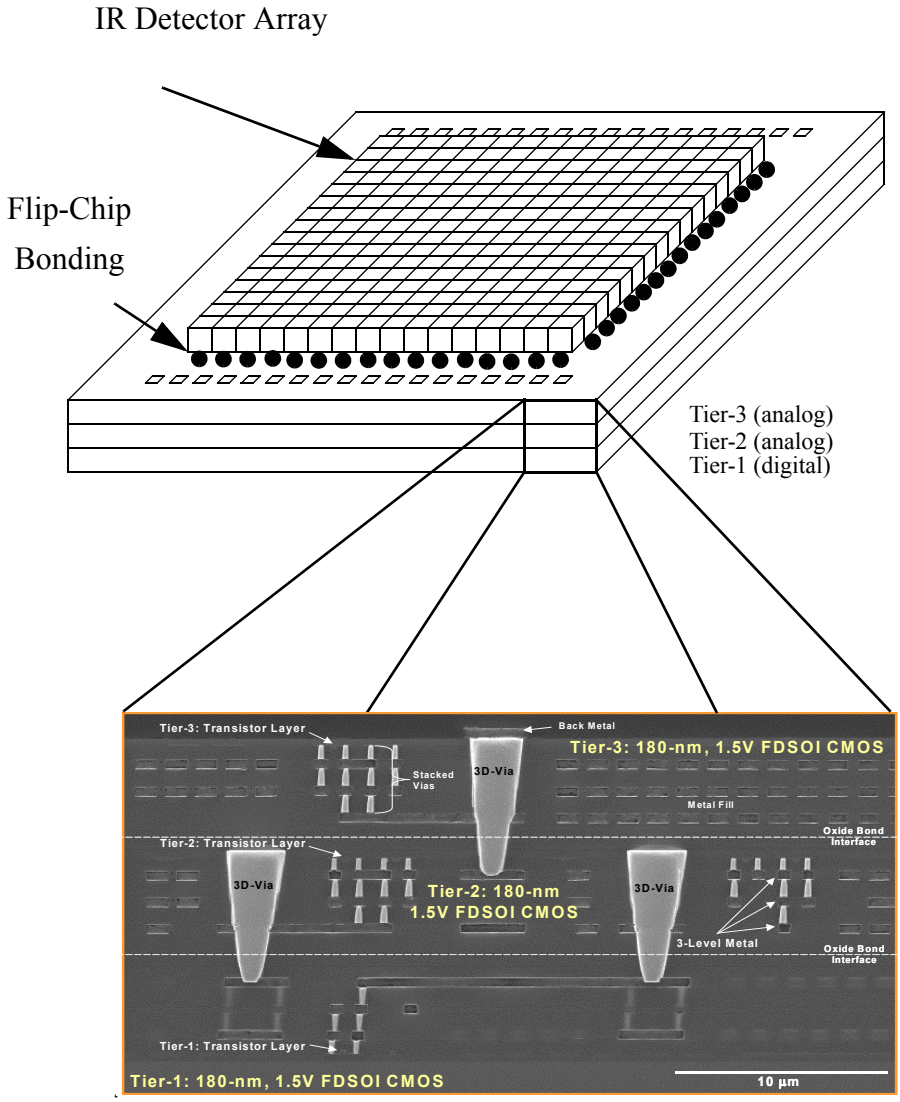


Figure 3.11: Vertically-integrated sensor array (VISA). Each circuit layer is fabricated, thinned, and bonded together. 3-D vias form electrical connections between different layers (Courtesy of MIT Lincoln Laboratory).

3.4 Per-Pixel Floating-Point Dual-Slope A/D Conversion

By using the 3-D IC technology described in Section 3.3, we can integrate an electronic shutter (a variable i_{ph}-to-V gain block) and a dual-slope ADC (a uniform ADC) within a pixel to implement a per-pixel floating-point dual-slope ADC. This section summarizes the requirements for an ADC for a high-frame rate and high-DR LWIR FPA and explains how a per-pixel floating-point dual-slope ADC architecture addresses those requirements.

First, the ADC must achieve a high frame rate and a high DR simultaneously and must be compatible with 3-D integration. Since a per-pixel implementation not only maximizes the number of converters, but also allows for per-pixel DR control, the per-pixel ADC is a suitable architecture for the high-frame rate and high-DR data conversion in LWIR FPAs. By using the through-wafer vias in the 3-D IC technology, the per-pixel ADC can easily be partitioned into multiple layers to reduce the pixel size.

Second, the ADC must dissipate low power because it is integrated with the LWIR detector array, which is operated at a cryogenic temperature. The maximum power dissipation of the ADC is limited by the capacity of the cooler. In this research, since the target power consumption of the ADC is 0.5 W for a 256 x 256 array, the power consumption of each per-pixel ADC must be less than 0.7 μW. A high frame rate and a high DR can be achieved with this low power consumption by using a floating-point ADC. Since the temperature resolution at high temperatures can be lower than at room temperature, the floating-point ADC architecture is a promising means of lowering the power consumption. This architecture preserves high resolution for the room temperature signals, while reducing the power consumption used to detect high temperature signals.

Third, the ADC must be small enough to fit within each pixel (50 x 50 μm^2 in this work), and mismatch among the ADCs must be small. Since the readout electronics for an IR FPAs already employ an integration capacitor to convert the photocurrent to the corresponding voltage, a current-mode dual-slope ADC can be implemented without much increase in area by adding a per-pixel discharge current source in each pixel. An additional

benefit of employing a dual-slope ADC is that it is straightforward to cancel mismatch among the per-pixel ADCs, as described in detail in Chapter 4.

3.5 Summary

In this chapter, a variety of on-focal-plane ADC architectures and per-pixel DR enhancement schemes have been reviewed. Compared with increasing the change-handling capacity, methods of changing the i_{ph}-to-V conversion gain offer a better trade-off between the DR and the frame rate because the former increases SNR and DR simultaneously, whereas the latter increases only the DR. The latter methods can be combined with a uniform ADC to construct a floating-point ADC.

Among the i_{ph}-to-V gain control methods, the overflow gate and the synchronous reset require the comparison level to vary within one frame. The multiple readout method requires a faster ADC and a frame buffer. The electronic shutter method uses a constant comparison level; furthermore, a comparator can be used instead of the fast ADC and frame buffer required in the multiple readout method. Therefore, integration time selection using electronic shutter appears to be the most promising for LWIR FPA application due to the relatively simple circuits required and the potential for low power implementation. By combining adaptive integration time control using an electronic shutter with a dual-slope ADC architecture, a power and area efficient per-pixel floating-point dual-slope ADC architecture can be implemented for high-frame rate and high-DR LWIR FPA applications. The detailed architecture for such an approach is described in Chapter 4.

Chapter

4

Per-Pixel Floating-Point Dual-Slope A/D Conversion

This chapter introduces the architecture of a per-pixel floating-point, dual-slope A/D converter (ADC) for a long wavelength infrared (LWIR) focal plane array (FPA) [26]. The use of a floating-point ADC architecture makes it possible to achieve a high frame rate and a high dynamic range simultaneously without large power consumption. The ADC architecture is based on a current-mode dual-slope ADC, and the floating-point feature is implemented using per-pixel electronic shutters. The electronic shutter is used to automatically control the integration time based on the detector current, and a per-pixel current source and a counter are used to measure the discharge time of the detector signal charge sampled at the end of different integration times.

The inverse of the selected integration time forms the exponent code, whereas the measured discharge time represents the mantissa code of the floating-point ADC. The name dual-slope ADC originates from these integration and discharge operations of the ADC. To improve the uniformity of the ADCs in the array, offset and gain errors are corrected using analog and digital methods. Being a per-pixel ADC, this architecture is easily scaled to larger array sizes and is well-suited to 3-dimensional (3-D) integration.

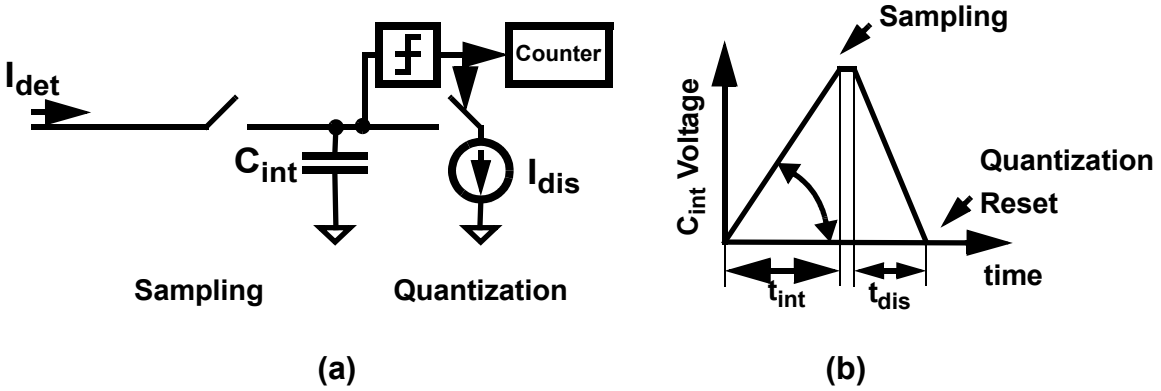


Figure 4.1: (a) Conventional dual-slope ADC and (b) its integration capacitor voltage waveforms.

Section 4.1 describes the architecture and operation of the proposed ADC. Section 4.2 explains mismatch correction techniques that reduce the gain and offset errors among the per-pixel ADCs. The chapter is summarized in Section 4.3.

4.1 Per-Pixel Floating-Point Dual-Slope ADC

4.1.1 Architecture

Figure 4.1 illustrates the architecture of a conventional current-mode, dual-slope ADC similar to that described in [47]. The input detector current is integrated onto the integration capacitor for a known integration time. Then, the capacitor is discharged by a known current source, while the discharge time is measured with a counter and a comparator. Because the same amount of charge is first integrated and then discharged, the input current is given by the discharge current multiplied by the ratio of the two times

$$I_{det} = I_{dis} \times \frac{t_{dis}}{t_{int}}, \tag{4.1}$$

where t_{int} is the known integration time, and t_{dis} is the quantized discharge time.

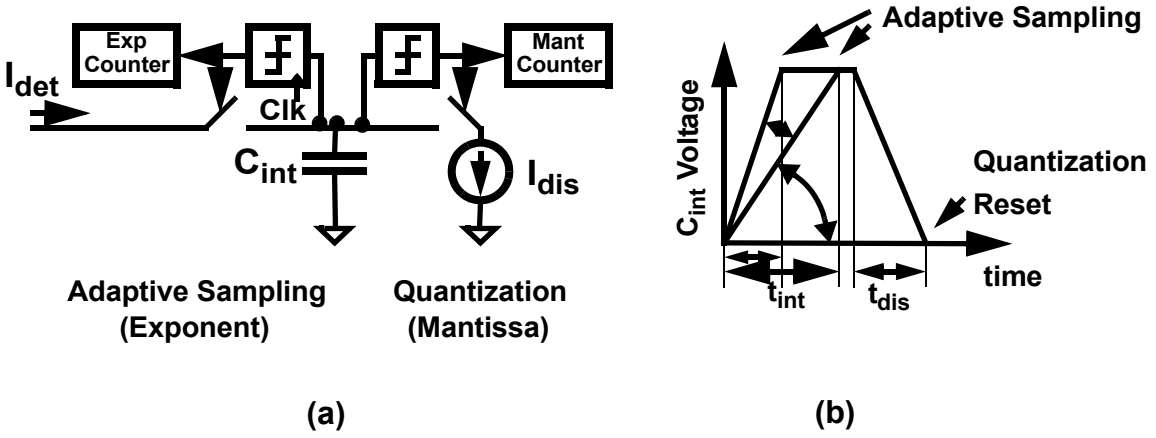


Figure 4.2: (a) Floating-point dual-slope ADC and (b) its integration capacitor voltage waveforms.

To increase the dynamic range of a dual-slope ADC, an electronic shutter that selects an integration time based on the amount of input current can be used [18]. Figure 4.2(a) shows a dual-slope ADC combined with an electronic shutter, an architecture that is referred to as a floating-point, dual-slope ADC in this research. The integration time of the shutter is controlled by an "exponent" counter and comparator that monitor the capacitor voltage. It is important to note that the possible integration times are restricted to a limited set of discrete times. By adapting the integration time to the input current, capacitor saturation is avoided, and the dynamic range is increased as shown in Figure 4.2(b). The inverse of the integration time ($1/t_{int}$) corresponds to the exponent and the discharge time (t_{dis}) to the mantissa in a floating point representation of the digitized detector current. To reduce the size of the ADC, the two counters can be shared among all pixels, and small memory blocks can be used to store the quantized integration and discharge times [17].

Figure 4.3 shows the proposed per-pixel floating-point, dual-slope ADC array architecture. Each pixel consists of a detector-biasing circuit, an integrator, a discharge circuit, and digital memory blocks. Clocks, counters, and digital readout circuits are shared by the entire pixel array.

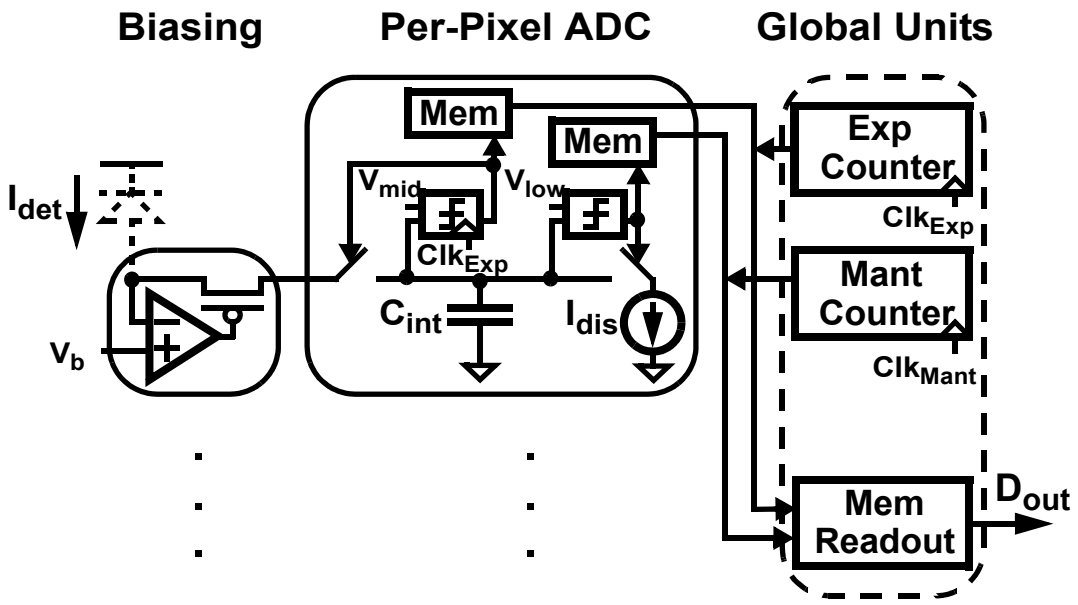


Figure 4.3: Per-pixel floating-point dual-slope ADC array.

4.1.2 Operation of ADC

The operation of the ADC is easily illustrated by referring to the waveforms of the integration capacitor shown in Figure 4.4.

At the beginning of the integration phase, the detector current is switched to the integration capacitor via an electronic shutter that is controlled by the exponent comparator, and the exponent counter begins counting. While the photocurrent from the detector is integrated onto the integration capacitor, the exponent comparator, which is strobed by the exponent clock, monitors the capacitor voltage. As shown in Figure 4.4 the exponent comparator terminates the integration at the first occurrence of the exponent clock pulse after the capacitor voltage rises above V_{mid}, the mid-point between V_{high} and V_{low}. At that instant, the exponent counter value is stored in the exponent memory. The use of exponentially-increasing integration times and the placement of the exponent comparator

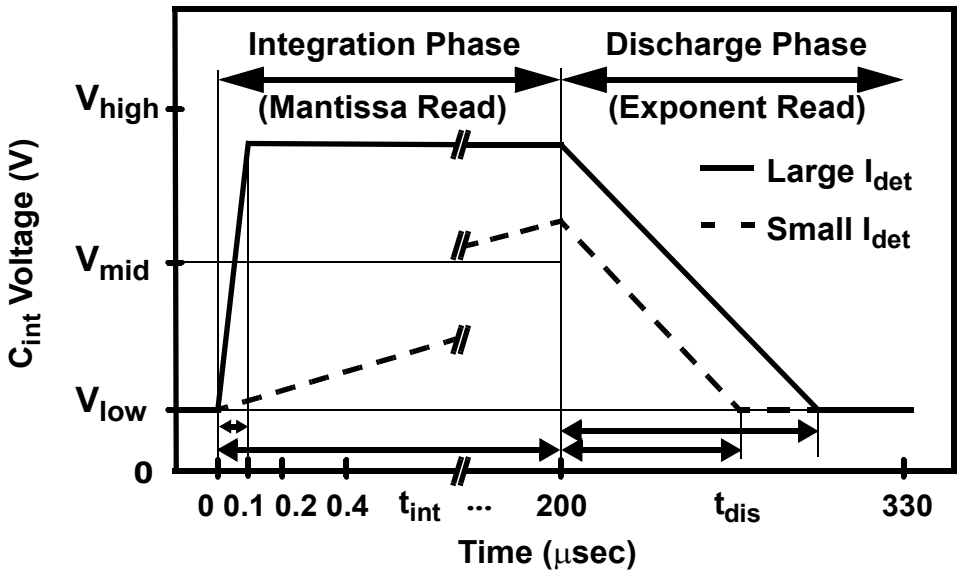


Figure 4.4: Integration capacitor voltage waveforms of floating-point dual-slope ADC.

threshold at V_{mid} guarantees that the capacitor voltage is sampled at the longest integration time that does not cause the capacitor to saturate [18].

For large photocurrents, a shorter integration time is selected to extend the dynamic range, whereas for smaller photocurrents, the use of a longer integration time makes it possible to resolve fine current differences. Because this approach relies on the capacitor voltage only to provide the coarse estimate needed to avoid saturation, there is no need for a precise, linear integration capacitor.

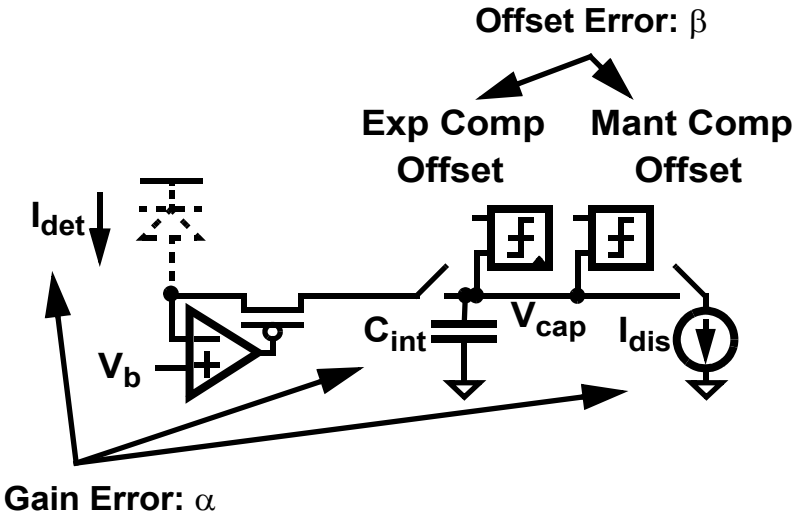
During the discharge phase, a constant current source discharges the integration capacitor, and the mantissa counter is activated. When the capacitor voltage returns to its initial value, the mantissa comparator stops the discharge operation, and the final counter value is stored in the mantissa memory. The digital exponent and mantissa values stored in the per-pixel memory blocks are read out during the discharge and integration phases, respectively, to pipeline the readout and, thus, achieve the maximum conversion rate.

4.2 Mismatch Correction

Mismatch among detector characteristics, comparator offsets, capacitance values, and discharging current sources will degrade the uniformity of the ADC array. As indicated in Figure 4.5, these mismatches can be modeled as gain and offset errors, which are denoted as α and β, respectively.

4.2.1 Exponent Comparator Offset Mismatch

Fortunately, offset mismatch among the exponent comparators merely alters the boundaries of the input ranges that are sampled at different sampling points, as illustrated in Figure 4.6. Therefore, this mismatch can be corrected by normalizing the digital outputs with only a small loss in resolution. For example, the two gray lines shown on the left and right in Figure 4.6 represent the same input signal. With offset, the input is sampled at 1/2 and generates an exponent and mantissa code pair of 2 and 01; without offset, the input is



$$I_{det} = \alpha\,(I_{dis} \times t_{dis}/t_{int}) + \beta$$

Figure 4.5: Potential sources of ADC mismatch.

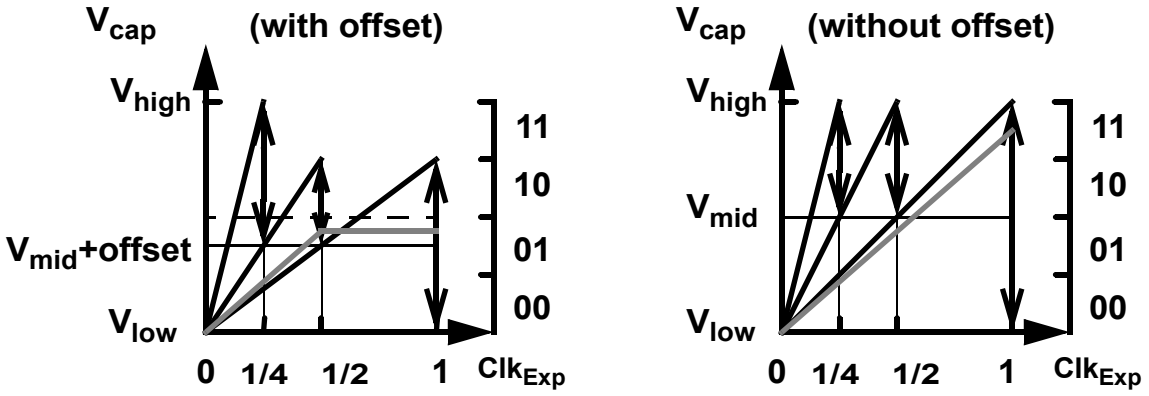


Figure 4.6: Effect of exponent comparator offset on ADC operation (Gray lines illustrate the same photocurrent sampled at different sampling points).

sampled at 1 and generates a pair of 1 and 11, which is normalized to an exponent of 2 and a mantissa of 01. Thus, offset in the exponent comparator only results in a small degradation in resolution.

4.2.2 Mantissa Comparator Offset Mismatch

On the other hand, offset mismatch in the mantissa comparators must be corrected in the analog domain since the offset directly affects the final mantissa code. Because the input common-mode voltage level and the discharging slope do not change over time, neither does the offset. Therefore, mantissa comparator offset can be cancelled by storing it on the integration capacitor at the end of the discharge phase and by starting the integration of the next frame from the stored voltage level as illustrated in Figure 4.7. This cancellation scheme also helps to suppress the effect of 1/f noise in the mantissa comparator.

The storage of the mantissa comparator offset is achieved by using a per-pixel current source and a continuous-time comparator rather than simply resetting the integration capacitor to a fixed voltage level. When the capacitor voltage drops below the sum of V_{low}

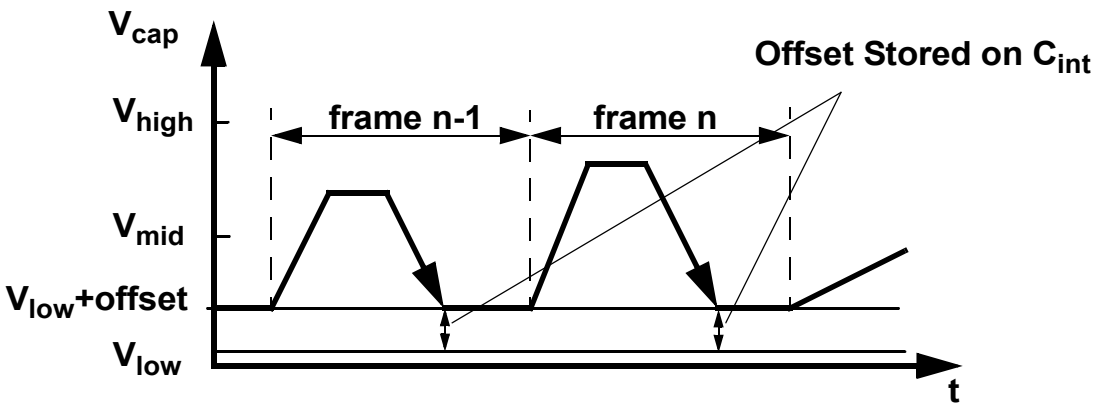


Figure 4.7: Effect of mantissa comparator offset on ADC operation.

and the offset (including 1/f noise), the comparator stops the discharge of the capacitor, and the comparator offset voltage is stored onto the capacitor. The use of a continuous-time comparator, rather than a clocked comparator, increases the voltage resolution of the offset cancellation because the comparator operation is not quantized in time. The continuous-time implementation also eliminates the need to distribute a high-speed clock to each pixel. The re-timing of the comparator output is done at the mantissa memory block using the transition edges of the mantissa counter outputs.

4.2.3 Gain Mismatch

As shown in Figure 4.8, with the offset error β resulting from the variation in the comparator offset corrected, only the gain error α resulting from mismatch among the detectors, the integration capacitors, and the discharging reference currents remains. The gain error can be corrected digitally using a multiplicative scaling factor for each pixel. The required scaling factors can be determined by shining a uniform light on the FPA.

4.3 Summary

This chapter presented the architecture of a proposed ADC for LWIR FPAs. The design employs per-pixel A/D conversion with an electronic shutter to achieve high frame rate

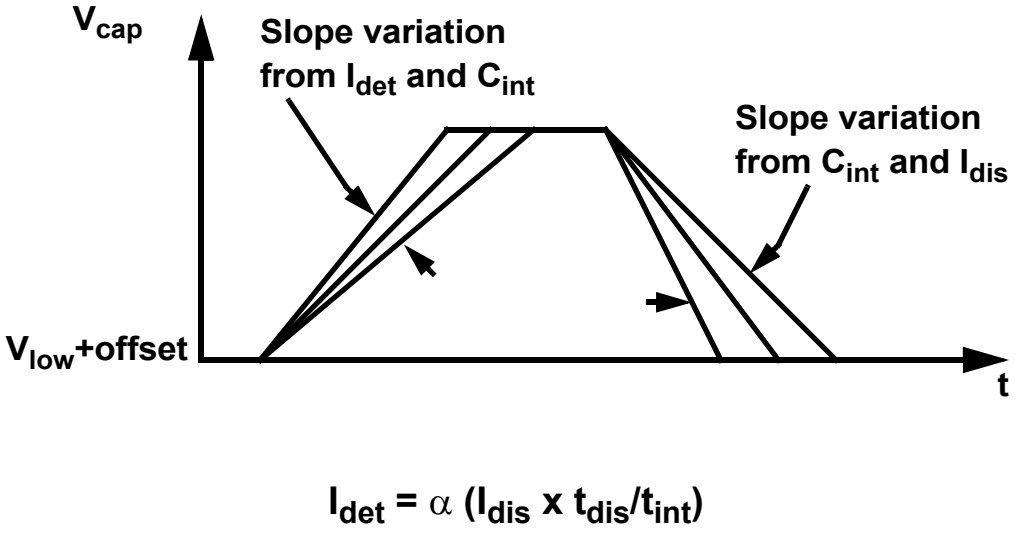


Figure 4.8: Effect of gain error after offset error corrected.

and high dynamic range simultaneously. The per-pixel ADC is based on dual-slope architecture to save area and power. The per-pixel electronic shutter automatically controls the integration time of each pixel based on the individual photo current. Thus, the integration capacitor is sampled at the longest integration time possible without saturating the capacitor. The integration time is selected from a discrete set of times and determines the exponent of the detector current. Fine conversion for the mantissa is then obtained by discharging the capacitor with a per-pixel current source and measuring the time until the capacitor is fully discharged. The different integration times correspond to different current-to-voltage gains required for floating-point A/D conversion. To improve the uniformity of the ADC array, a comparator offset cancellation scheme using integration capacitor is proposed. This scheme not only cancels pixel-to-pixel comparator offset, but also reduces 1/f noise.

Chapter 5

Circuit Implementation

This chapter describes the circuit design for the proposed per-pixel floating-point dual-slope ADC array. Shown in Figure 5.1 is a block diagram of a 16 x 16 prototype ADC array. The pixel circuits convert the input photocurrent into digital exponent and mantissa codes and stores these codes in per-pixel digital memory. The peripheral circuits

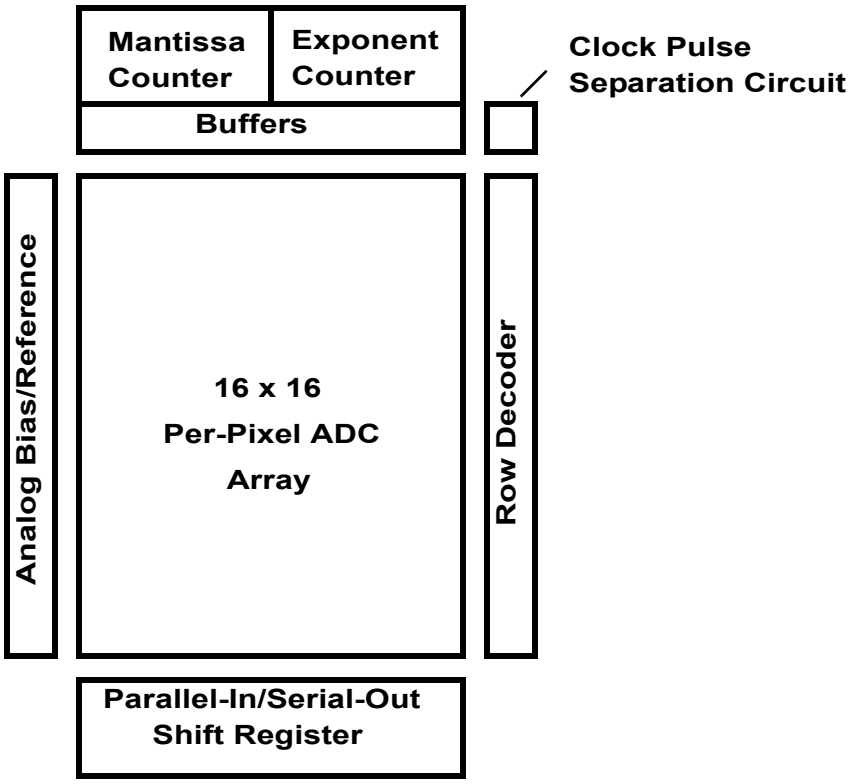


Figure 5.1: Block diagram of prototype ADC array.

provide analog bias/reference voltages, counter values, and control signals to each pixel, and read out the exponent and mantissa codes stored in the per-pixel memory.

Section 5.1 presents a summary of noise considerations for the per-pixel ADCs, which provides a guideline for the design. Sections 5.2 and 5.3 describe the pixel and peripheral circuits, respectively, and Section 5.4 summarizes the chapter.

5.1 Noise Analysis

As indicated in Figure 5.2, there are several sources of noise to consider in the design of the per-pixel floating-point dual-slope ADC: photon shot noise, thermal noise, 1/f noise, and reference noise.

5.1.1 Photon Shot Noise

The photon shot noise is generated by the random fluctuation in the number of the generated electrons in response to the incident photons at the detector [1]. Since this noise can be described by a Poisson distribution, the photon shot noise at the end of the integration is

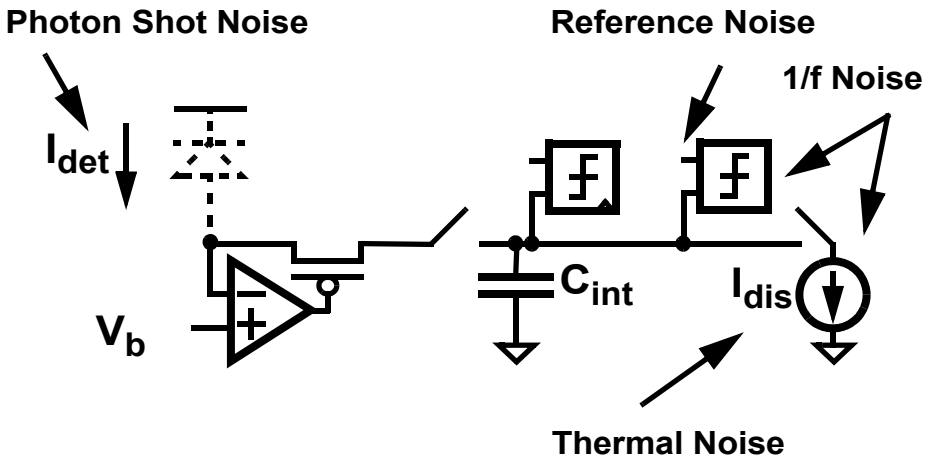


Figure 5.2: Major sources of noise.

proportional to the amount of charge stored on the integration capacitor. The shot noise is stored on the integration capacitance, C_{int}, as a voltage, and the noise power is

$$\overline{V_{shot}^2} = \frac{qi_{ph}t_{int}}{C_{int}^2} = \frac{qC_{int}V}{C_{int}^2} \leq \frac{qV_{max}}{C_{int}}, \tag{5.1}$$

where q is the electron charge of 1.602 x 10^{-19} C, i_{ph} is the photocurrent, t_{int} is the integration time, V is the integrator output voltage, and V_{max} is the maximum integrator swing.

5.1.2 Thermal Noise

The per-pixel current source and the switch that connects the current source and the integration capacitor generate thermal noise during the discharge phase, which is accumulated onto the capacitor as a voltage. Figure 5.3 is the equivalent circuit model used during the discharge phase for thermal noise calculations. To simplify the derivation, the switch noise and the current source non-ideality, such as non-zero output conductance, have been ignored in the model, which does not significantly alter the final result.

If the per-pixel current source, I_{dis}, in Figure 5.2 is implemented with an MOS transistor, then the one-sided current noise power of the current source is given by

$$\overline{I_{therm}^2} = 4kT\gamma g_m \Delta f, \tag{5.2}$$

Figure 5.3: Equivalent circuit during discharge for thermal noise calculation.

where γ is a parameter that depends on the channel length and the biasing conditions of the transistor, and g_m is the transconductance of the transistor [48]. This current noise is integrated onto the capacitor only during the discharge time, t_{dis}. Because the Fourier transform of the impulse response of a time limited integration is a sinc function [49], [50], the thermal noise power integrated onto the capacitor during the discharge time can be calculated in frequency domain as

$$\overline{V_{therm}^2} \approx \frac{4kT\gamma g_m}{C_{int}^2}\int_0^\infty \left(t_{dis}\frac{\sin(\pi t_{dis} f)}{(\pi t_{dis} f)}\right)^2 df = 2kT\gamma g_m \frac{t_{dis}}{C_{int}^2}. \quad (5.3)$$

The approximation sign is due to the assumption of an ideal switch and an ideal current source.

5.1.3 1/f Noise

The 1/f noise of the mantissa comparator and discharge current source can be reduced by increasing their transistor sizes, although it is difficult to increase them due to the limited pixel size. It has been reported that by switching the current source on and off, the 1/f noise of current source below the switching frequency can be reduced [51]. The mantissa comparator offset cancellation scheme explained in Chapter 4 has the similar effect of reducing the 1/f noise of the current source, as well as that of the mantissa comparator below the frequency of offset cancellation cycle. This can be explained intuitively as follows. If the frequency of the offset cancellation is higher than that of 1/f noise, the correlation between the two consecutive samples used for the offset cancellation is high; thus, the offset cancellation reduces the 1/f noise. As the frequency of 1/f noise becomes higher compared with that of the offset cancellation, the correlation of the two samples becomes lower; thus, the noise reduction becomes smaller.

5.1.4 Reference Noise

Any type of noise coupled to the analog reference voltage for the mantissa comparator directly degrades the mantissa resolution of the ADC. Therefore, care must be taken in the

design of the analog reference voltages and their distribution. On-chip reference voltage generation would be a better choice for reducing the noise coupling; however, the prototype ADC array uses external reference voltages for testing flexibility.

5.2 Pixel Circuits

Shown in Figure 5.4 are the per-pixel circuits, which include a PMOS cascode current source, an integration capacitor, a BDI circuit with an electronic shutter, a discharge current source, exponent and mantissa comparators, and digital memory blocks.

The photovoltaic (PV) HgCdTe LWIR detector for which the per-pixel ADC is designed has the following characteristics. The absorption band is from 7.8 μm to 10.5 μm, and the quantum efficiency is 0.85. Assuming an f-number of 2.5, an optical transmission of 1, a fill factor of 0.925, and a detector size of 50 x 50 μm^2, we can calculate the photocurrent of the detector using Equation (2.5) in Chapter 2. Table 5.1 shows the calculated photocurrents of the LWIR detector for several different temperatures.

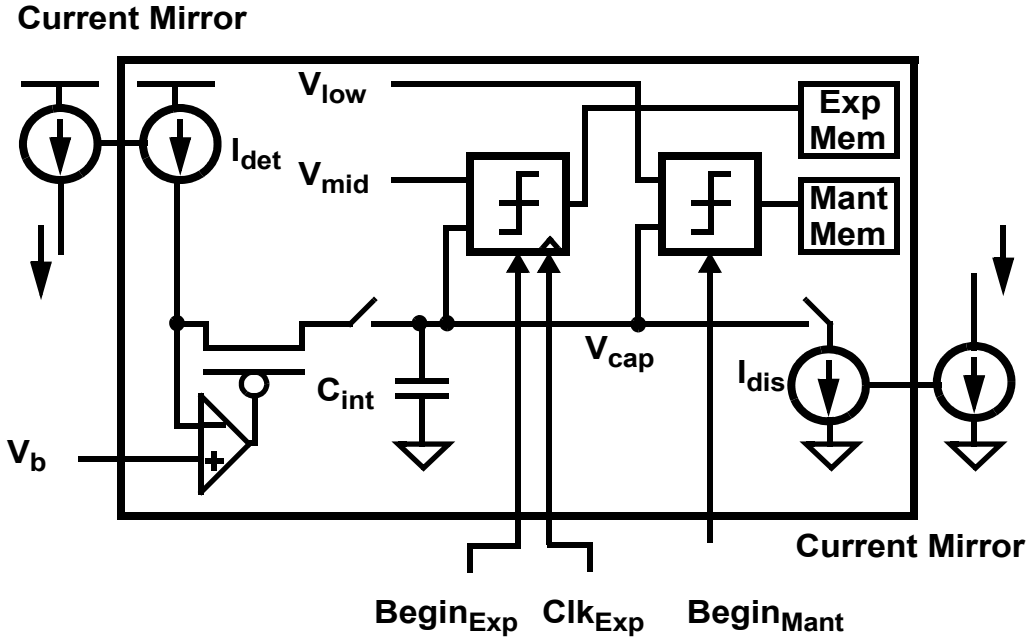


Figure 5.4: Block diagram of a pixel circuit.

Temperature	270 K	280 K	290 K	300 K	310 K	9000 K
Photocurrent	26.7 nA	32.9 nA	39.8 nA	47.8 nA	56.6 nA	49.9 μA

Table 5.1 Photocurrents of LWIR detector for different temperatures.

The prototype floating-point ADC is designed to accommodate a temperature range from 270 K to 9000 K (a photocurret range from 25 nA to 50 μA) and to achieve a temperature resolution of 0.2 K at 270 K (a current resolution of 0.1 nA for a 25 nA range). This target can be achieved by designing a floating-point ADC with an 11-bit exponent and an 8-bit mantissa.

5.2.1 Per-Pixel Current Source Emulating LWIR Detector

Due to practical difficulties of employing an actual LWIR detector array in testing the prototype ADC array, a PMOS cascode current mirror, shown in Figure 5.5, that emulates LWIR detector current is implemented in each pixel. To bias the current mirror for a wide range of currents from 25 nA to 50 μA, a higher supply voltage was used for the current mirror: 3.3 V in 2-D implementation and 2.5 V in 3-D implementation, instead of 1.8 V and 1.5 V, respectively. The transistor size of both the current source and cascode devices is W/L = 4.2 μm/420 nm for the 2-D chip and W/L = 8 μm/400 nm for the 3-D chip.

In addition to the normal pixels with the PMOS current mirror, test pixels without the current mirror whose input current is directly supplied by an external current source were

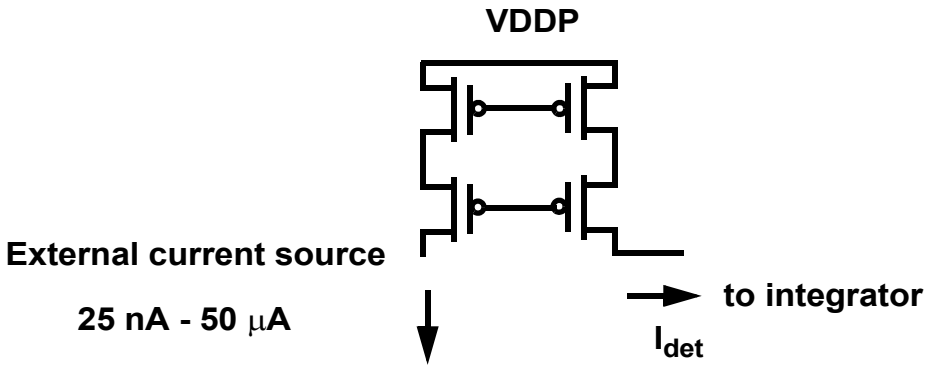


Figure 5.5: Per-pixel PMOS current source.

also included in the 16 x 16 array in order to characterize the ADC more accurately, as described in detail in Chapter 7.

5.2.2 Integration Capacitor

Unlike CMOS visible sensors, LWIR detectors must detect a small temperature difference in the presence of a large background temperature radiation. Therefore, a large integration capacitor is typically used in LWIR imaging to increase the charge-handling capacity and, thus, the signal-to-photon shot noise ratio. Employing a large capacitance also helps to reduce the thermal noise of the per-pixel current source in the proposed ADC.

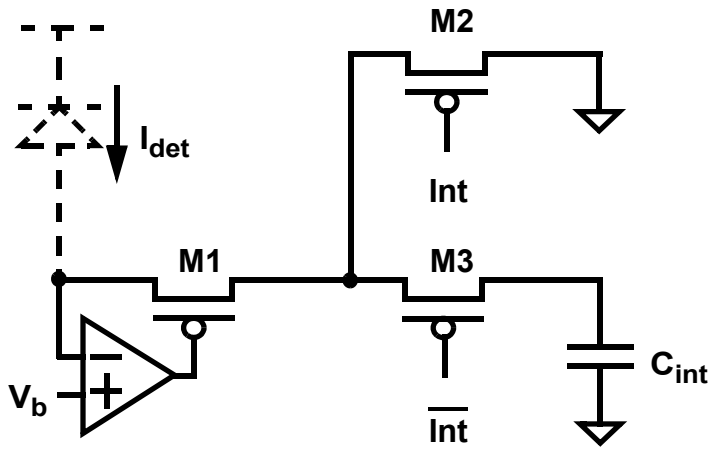
The shot noise and thermal noise can be calculated from Equations (5.1) and (5.3), respectively. Calculated noise values for several different capacitance values are tabulated in Table 5.2, assuming a discharge time, t_{dis}, of 60 μsec, g_m of 1 mS, γ of 1/2, and a maximum integrator swing, V_{max}, of 0.8 V. These results reveal that the thermal noise of the per-pixel current source dominates over the photon shot noise. In the prototype, a capacitance of ~6 pF was chosen to achieve an SNR of ~9 bits at a 70-K operating temperature (and ~8 bits at a 300-K measurement temperature of the prototype). Because the proposed ADC topology does not require a linear integrator, the large integration capacitance has been realized in a relatively small area using an MOS accumulation capacitor.

capacitance	0.75 pF	1.5 pF	3 pF	6 pF
shot noise	0.413 mV_{rms}	0.292 mV_{rms}	0.207 mV_{rms}	0.146 mV_{rms}
thermal noise @ 70 K	10.5 mV_{rms}	5.25 mV_{rms}	2.62 mV_{rms}	1.31 mV_{rms}
swing/(shot noise + thermal noise @ 70 K)	78	157	314	626 (~9 bits)
thermal noise @ 300 K	21.0 mV_{rms}	10.5 mV_{rms}	5.25 mV_{rms}	2.63 mV_{rms}
swing/(shot noise + thermal noise @ 300 K)	38	76	152	304 (~8 bits)

Table 5.2 Shot and thermal noise voltages and signal-to-noise voltage ratios with a maximum integrator swing of 0.8 V for several integration capacitances.

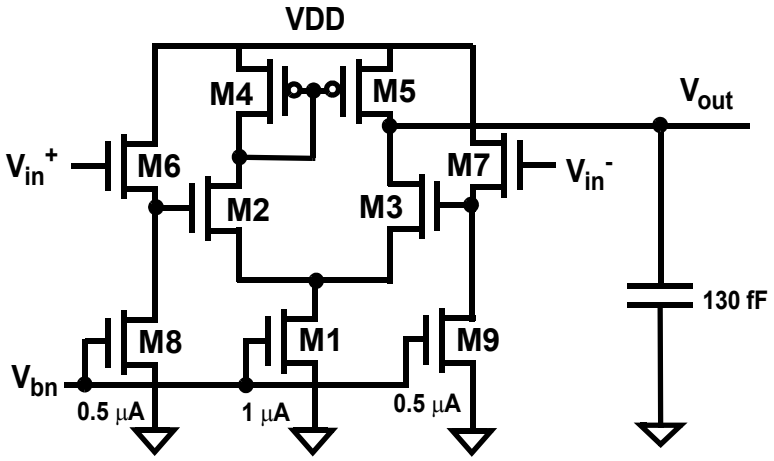
5.2.3 BDI with Electronic Shutter

As shown in Figure 5.6, the prototype array employs buffered direct injection (BDI) [41] in each pixel as a detector interface circuit to improve the efficiency of the injection of the detector current onto the integration capacitor and provide a stable bias for the LWIR detector over a large signal dynamic range (25 nA - 50 μA) with low power dissipation. The bias current of the operational amplifier (op-amp) need not be as large as the maximum detector current, as is the case in a transimpedance amplifier used in an integrator, since the amplifier need only drive the common-gate buffer rather than a large integration capacitance. To minimize voltage fluctuations at the detector biasing node, the detector current is steered to ground when it is not being integrated. The two types of op-amp used for the BDI circuits in 2-D and 3-D prototypes, respectively, are shown in Figure 5.7 with appropriate values of compensation capacitances.

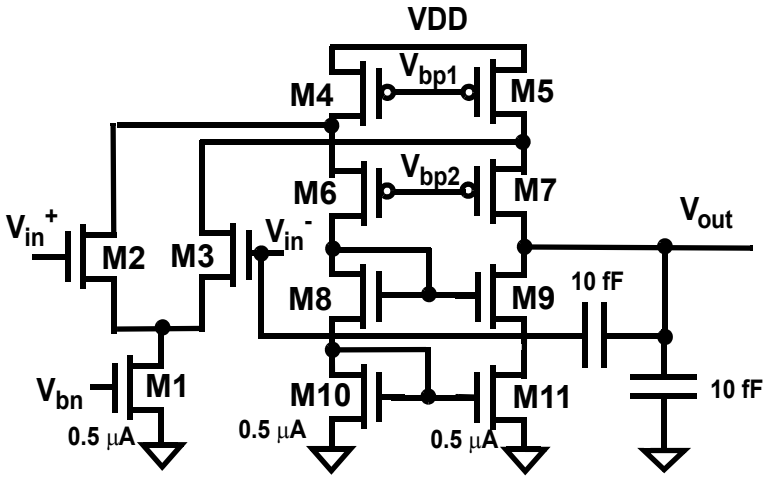


	2-D	3-D
M1	3μ/300n	2μ/200n
M2, M3	280n/600n	700n/800n

Figure 5.6: BDI with electronic shutter.



(a)



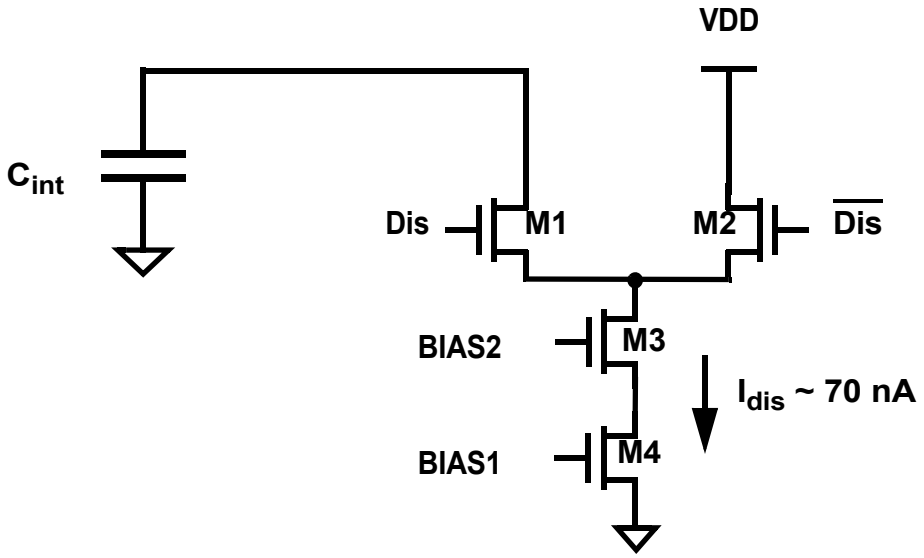
(b)

	2-D	3-D
M1	4μ/400n	600n/420n
M2, M3	4μ/1.6μ	20μ/700n
M4, M5	4μ/1.6μ	600n/420n
M6, M7	1μ/3.3μ	600n/420n
M8, M9	1μ/400n	600n/420n
M10, M11		600n/420n

Figure 5.7: Op-amps in BDI for (a) 2-D prototype and (b) 3-D prototype.

5.2.4 Discharge Current Source

In each pixel, a nominal 70-nA current source, mirrored from a master current source, is used to discharge the integration capacitor. To keep the discharge slope fairly constant, a cascode current source is used, as shown in Figure 5.8. A larger than minimum channel length is used for the current source transistor to improve the matching among these devices. While a large gate overdrive voltage on the current source (small g_m) is appropriate for matching, noise, and output impedance, it would reduce voltage swing and, thus, limit the ADC resolution, especially in the 3-D prototype with a 1.5-V supply voltage. To reduce glitches during the switching, complementary switches are employed, and to reduce the bias fluctuation de-coupling capacitance is attached to the current source bias lines. Current source mismatch is corrected in the digital domain.



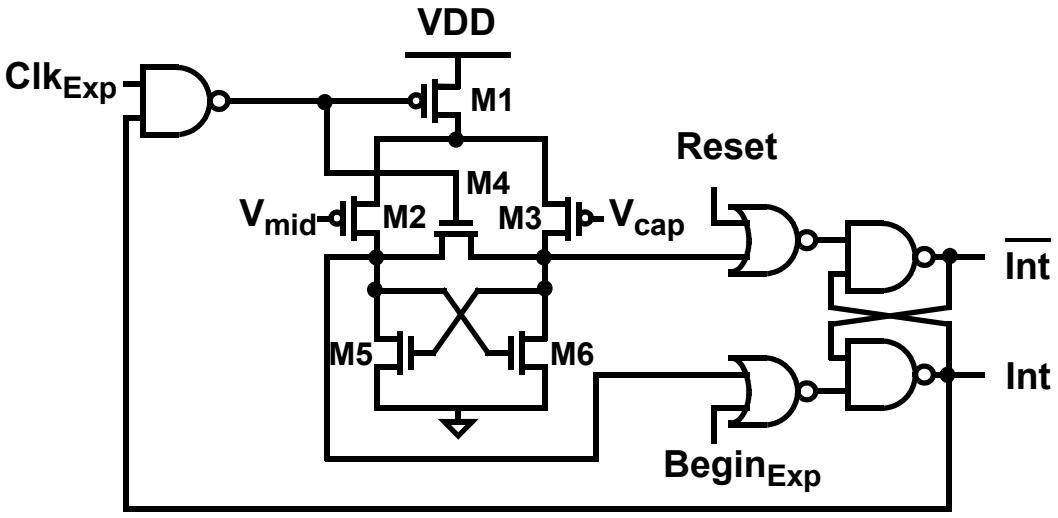
	2-D	3-D
M1, M2	280n/380n	700n/800n
M3	560n/3µ	2µ/400n
M4	560n/3µ	2µ/400n

Figure 5.8: Discharge current source.

5.2.5 Exponent and Mantissa Comparators

The exponent comparator controls the electronic shutter that determines the integration times. To accurately achieve exponentially increasing integration times, delay variations of the comparator resulting from integrator voltage slope variation must be minimized. To achieve a small delay variation without much increase in area and power dissipation, the exponent comparator, shown in Figure 5.9, is implemented as a simple regenerative latch, clocked by the exponent clock, followed by an SR latch. Because the number of the comparison needed to achieve an 11-bit exponent is only twelve, clock feed through in the comparator does not significantly disturb the integrator and reference voltages.

Unlike the exponent comparator, the mantissa comparator must monitor the crossing of the capacitor voltage across the reference, V_{low}, much more frequently (2^8 times for 8-bit



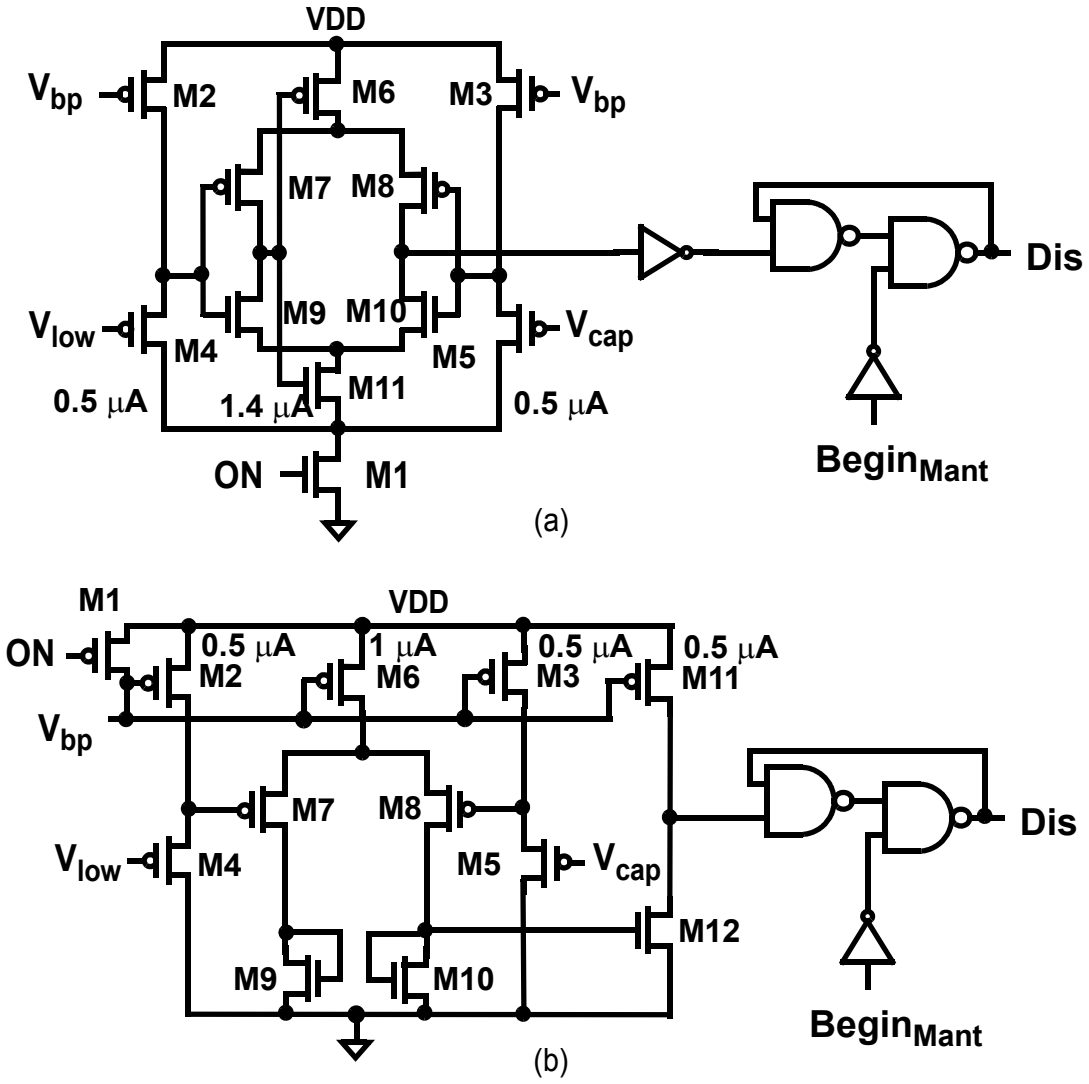
	2-D	3-D
M1	2.5µ/600n	3µ/200n
M2, M3	12.6µ/600n	5µ/200n
M4	2.2µ/600n	950n/200n
M5, M6	4µ/600n	1.6µ/200n

Figure 5.9: Exponent comparator.

mantissa resolution) than the exponent comparator crosses the reference, V_{mid} (12 times for 11-bit exponent) to measure the discharge time. Because of this large number of comparisons, a clocked mantissa comparator would increase power dissipation and disturb the integrator and reference voltages with much more clock feed through. In addition, the disturbance of the reference voltage from neighboring comparators that share the same reference must be reduced.

To address these issues, the mantissa comparator is implemented with a continuous-time comparator. As illustrated in Figure 5.10, a self-biased differential amplifier [52] is used for the 2-D chip, and a simple differential pair is used for the 3-D chip. To accommodate low input common-mode ranges close to V_{low}, PMOS source followers are used to level shift the comparator inputs. The average power dissipation is reduced by activating the comparator with the switch M1 only during the discharge phase. The gain of the comparator is kept small to ensure that the comparator has a sufficiently fast recovery time relative to the discharge voltage slope. As a result, both the operating point and the delay of the comparator at the trip point are independent of the magnitude of the voltage sampled on the integration capacitor. It is important that the comparator delay be invariant from frame to frame if the offset cancellation scheme explained in Chapter 4 is to function correctly.

In the operation of the exponent comparator during the integration phase, because the exponent clock pulses are active even after the sampling of a large photocurrent, any leakage from the integrator or kickback noise from the comparator could reactivate the comparator and store an incorrect time stamp in the local exponent memory. Similar incorrect operation of the mantissa comparator can occur during the discharge phase because the mantissa comparator is active throughout the discharge phase. To prevent possible multiple sampling of the integration capacitor, both exponent and mantissa comparators employ a designated begin signal ($Begin_{Exp}$ and $Begin_{Mant}$ in Figures 5.9 and 5.10) and digital logic that prevents multiple switching during a single conversion cycle.



	2-D	3-D
M1	280n/180n	2μ/200n
M2, M3	440n/4μ	1μ/400n
M4, M5	1μ/180n	1μ/200n
M6	280n/4μ	2μ/400n
M7, M8	2.4μ/180n	1μ/200n
M9, M10	2.4μ/180n	1μ/2μ
M11	280n/4μ	1μ/400n
M12		1μ/400n

Figure 5.10: Mantissa comparators for (a) 2-D prototype and (b) 3-D prototype.

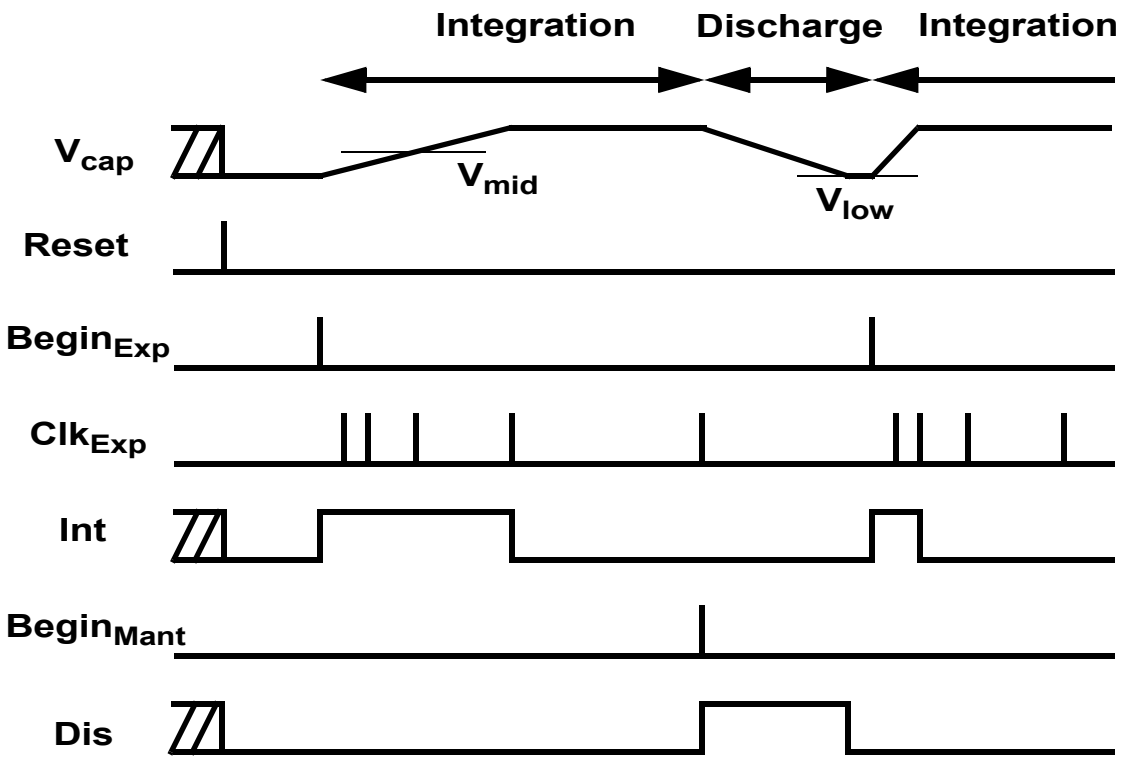
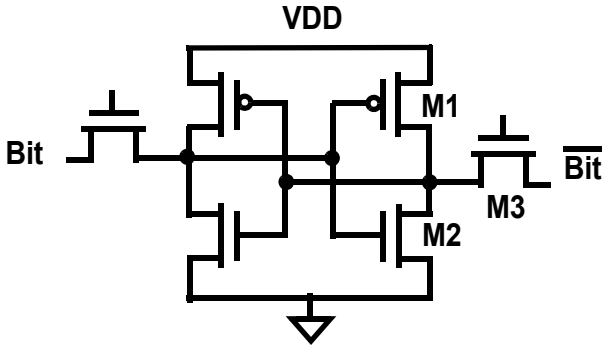


Figure 5.11: Timing diagram of ADC operation with digital logics that prevent multiple switching of exponent and mantissa comparators.

A timing diagram for the control of the exponent and mantissa comparators is shown in Figure 5.11. The Reset signal initializes the states of the integrator and two comparators at the power up of the chip. During the integration phase, a $Begin_{Exp}$ pulse initiates the integration and enables the Clk_{Exp} path to the comparator (shown in Figure 5.9). When the exponent comparator output switches, and, thus, the Int signal goes low, Clk_{Exp} to the exponent comparator is blocked, and further switching of the comparator is disabled. Similarly, during the discharge phase, a $Begin_{Mant}$ pulse initiates the discharge. Once the mantissa comparator switches, and, thus, the Dis signal becomes low, further switching of the comparator is disabled. The generation of the Begin pulse from the original clock is described in Section 5.3.



	2-D	3-D
M1	600n/180n	600n/200n
M2	1.6μ/180n	1.6μ/200n
M3	1.6μ/180n	1.6μ/200n

Figure 5.12: SRAM.

5.2.6 Per-Pixel Memory

To store the exponent and mantissa codes, two blocks of memory are implemented in each pixel. The six-transistor one-port SRAM cell shown in Figure 5.12 is used to implement the memory. Four bits are assigned to the exponent to represent 11 ($< 2^4$) different mantissa codes, and 16 bits are assigned to the mantissa to measure the sub-LSB resolution of the mantissa.

At the beginning of the integration or discharge phase, M3 is turned on, and the exponent or mantissa counter begins to write its output to the memory. As soon as the exponent or mantissa comparator switches, M3 is turned off, which samples the counter value written in the memory at that moment. M3 is turned on again during the exponent or mantissa readout cycle.

5.3 Peripheral Circuits

This section describes the circuit blocks that are shared by the 16 x 16 ADC array.

5.3.1 Bias and Reference Voltages

The bias voltages for the op-amp in the BDI circuit, the mantissa comparator, the PMOS cascode current source, and the discharge current source are generated by feeding external

currents to master current mirror circuits implemented on chip, whereas the reference voltages for the exponent and the mantissa comparators are generated off chip. The bias and reference voltages are routed to the entire array. Bypass capacitors are used for the bias and reference routing.

5.3.2 Exponent and Mantissa Counters

Gray counters [53] are used for both 4-bit exponent and 16-bit mantissa counters to reduce bit errors during the sampling of the counter values onto the per-pixel memory. The use of a Gray counter is especially helpful in reducing bit errors for the mantissa counter because the switching of the mantissa comparator can occur at the transition of the counter output since the switching is not synchronized with the counter clock. The outputs of counters are buffered to drive the large capacitive load presented by the per-pixel memory in the 16 x 16 ADC array.

5.3.3 Clock Pulse Separation Circuit

The exponent and mantissa clocks are generated by an off-chip FPGA board and a bench-top pulse generator, respectively. The first and the remainder pulses need to be separated because they are used for different purposes, as explained in Section 5.2.5. The first pulse (Begin) is used to reset the counters and initiate the integration/discharge of the per-pixel ADCs, whereas the remainder pulses are used to clock the counters and to stop the integration.

Instead of separating the pulses off-chip and routing them using two different paths, the pulse is separated on chip just before they are fed to the counters and the ADC array in order to minimize the skew resulting from different path delays. Figure 5.13 illustrates the on-chip circuitry used to separate the first and remainder pulses. The circuit separates the first pulse following the rising edge of the En signal from the subsequent pulses. It employs positive and negative edge-triggered flip-flops that are initialized by a power-on reset signal.

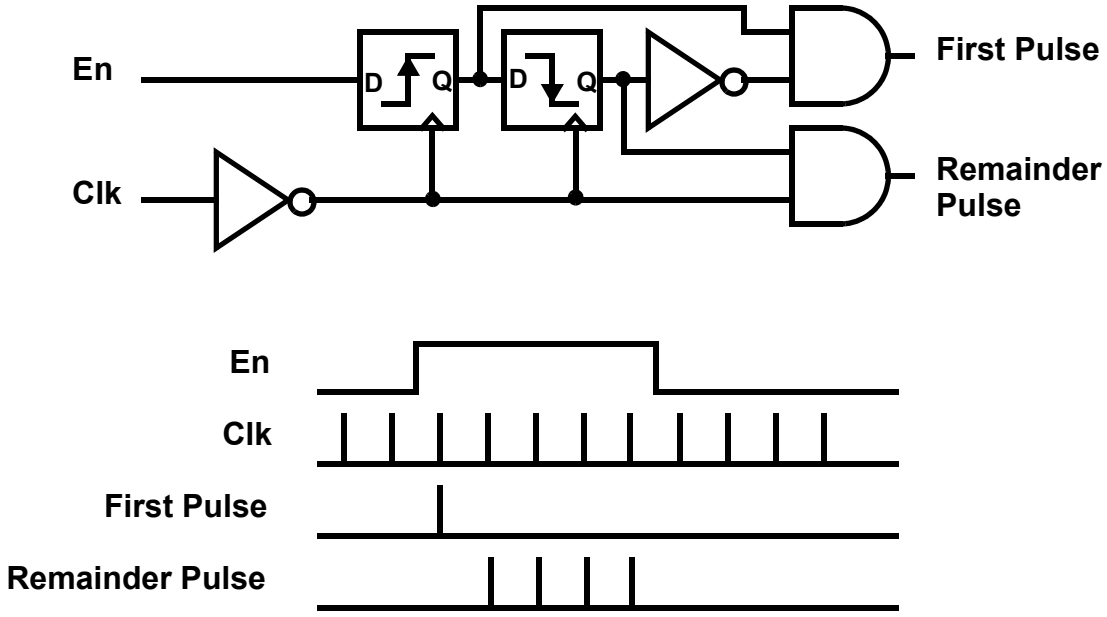


Figure 5.13: Clock pulse separation circuit.

5.3.4 Memory Readout Circuit

The row decoder of the memory readout circuitry shown in Figure 5.1 is implemented using a shift register, which is initialized by Reset signal to point to the top row. Figure 5.14 illustrates a timing diagram used for the exponent and mantissa readout. The row decoder can be set to increment synchronously with Clk_{Row}. When Clk_{Load} is high, the 16

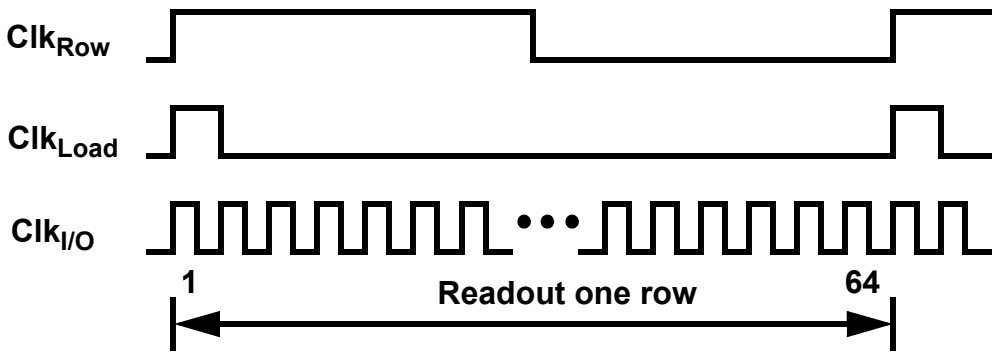


Figure 5.14: Timing diagram of memory readout.

exponents or 16 mantissas of one row (for 16 ADCs) are transferred from per-pixel memory to 16 4-in/1-out shift registers or 16 16-in/4-out shift registers, respectively. It takes 64 cycles (=16 x 4) of $Clk_{I/O}$ signal to read the 16 exponents (or 16 mantissas) in the shift register through the I/O pads (one I/O pad for the exponent and four I/O pads for the mantissa). To read either the mantissas or the exponents of the entire 16 x 16 ADC array, it takes 16 x 64 cycles of $Clk_{I/O}$ signal.

5.4 Summary

This chapter describes circuit design details for the proposed ADC. Noise analysis of the ADC shows that the mantissa resolution of the ADC is limited by thermal noise of the per-pixel current source. A large integration capacitor is employed to increase the mantissa resolution. The design is targeted to achieve an 8-bit mantissa resolution at 300 K and an 11-bit exponent, providing a 19-bit dynamic range for an LWIR detector whose current ranges from 25 nA to 50 μA. Efforts have been made to minimize the power dissipation and size of the circuits.

Chapter

6

2-D and 3-D Experimental Prototypes

This chapter describes two prototype chips fabricated in 2-D and 3-D technologies, respectively, to demonstrate the potential of the proposed ADC architecture and the feasibility of pixel size reduction using 3-D integration. The first prototype was integrated in a 2-D, single-poly, five-metal, 0.18-μm CMOS technology and operates from a 1.8-V supply. The second prototype was integrated in a 3-D, single-poly, three-metal, 0.18-μm fully-depleted silicon-on-insulator (FDSOI) technology and operates from a 1.5-V supply. For both prototypes, the 16 x 16 per-pixel ADC array and the circuits described in Chapter 5 were implemented on chip. For testing flexibility, control signals for the prototypes are generated off-chip using a filed programmable gate array (FPGA) board, and reference voltages for the comparators are generated using off-chip circuitry on the test board. Details of the test setup are described in Chapter 7.

Section 6.1 describes the 2-D prototype. Section 6.2 describes the 3-D FDSOI technology of the MIT Lincoln Laboratory, and Section 6.3 describes the 3-D prototype. Section 6.4 summarizes the chapter.

6.1 2-D Prototype in CMOS

A micrograph of the 2-D chip is shown in Figure 6.1. The total chip size is 2.1 x 2.3 mm^2, and the area of one pixel is 4000 μm^2. The 16 x 16 per-pixel ADC array is located in the

center of the chip. The exponent and mantissa counters and the digital buffers are placed at the top of the ADC array, and the analog bias generators are located on the left side of the array. The row decoder and the parallel-in-serial-out shift register used for the SRAM readout are located on the right side and at the bottom of the ADC array, respectively. To accommodate the large number of I/O pads in the limited area, we used staggered pads.

Care was taken in the on-chip analog and digital signal routing to minimize the coupling of digital switching noise into sensitive analog circuits. Separate analog and digital grounds are used. In analog circuit regions, the substrate is connected to the analog ground, whereas in digital regions the substrate is not connected to ground, but is routed to a separate bond pad to minimize the digital noise injection into the low-resistance substrate of the epitaxial technology. The back side of the chip was directly bonded to the package ground to achieve a good substrate-to-ground contact. Referring to Figure 6.1, the digital counter outputs are routed from the top of the chip using metal 3. Digital control signals are distributed from the right using metal 4, while the analog bias lines are distributed from the left using metal 5. Bypass capacitance for the digital power supply is located on the right side of the array, while that for the analog bias and reference voltages is on the left side.

The detailed layout of the per-pixel ADC is shown in Figure 6.2. The top half is composed of the analog circuits and analog bias lines (metal 5) running horizontally above the analog circuits. The BDI circuit and the PMOS current source that emulates LWIR detector current are placed on the top left side of the pixel. The 6-pF integration capacitor is located at the top right of the pixel. Additional bypass capacitors are placed in each pixel for the analog bias and reference voltages, and a metal shield (metal 2) connected to the digital substrate terminal is used to protect the integration capacitor from the digital routing (metal 3) from the counters.

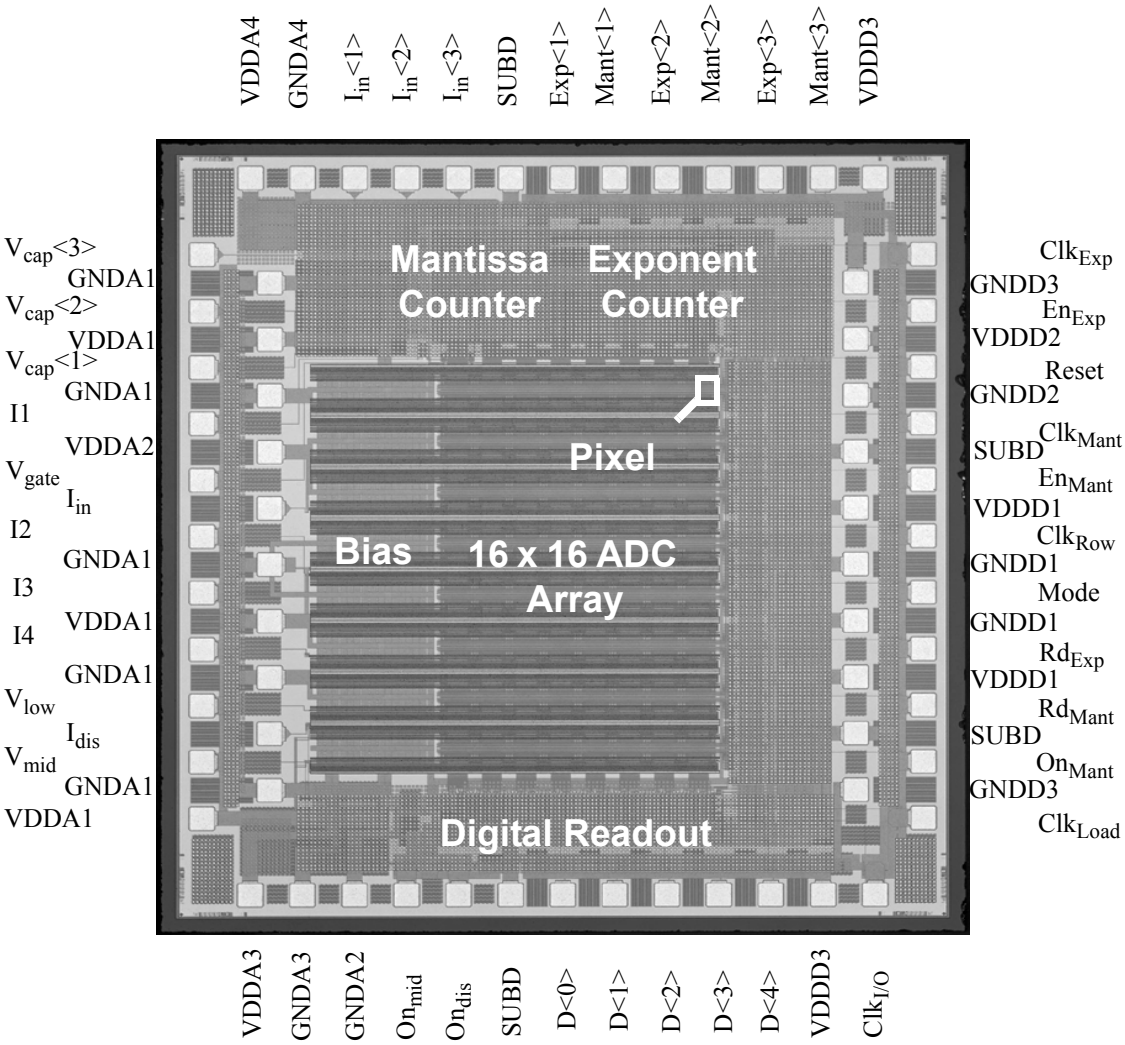


Figure 6.1: 2-D chip micrograph.

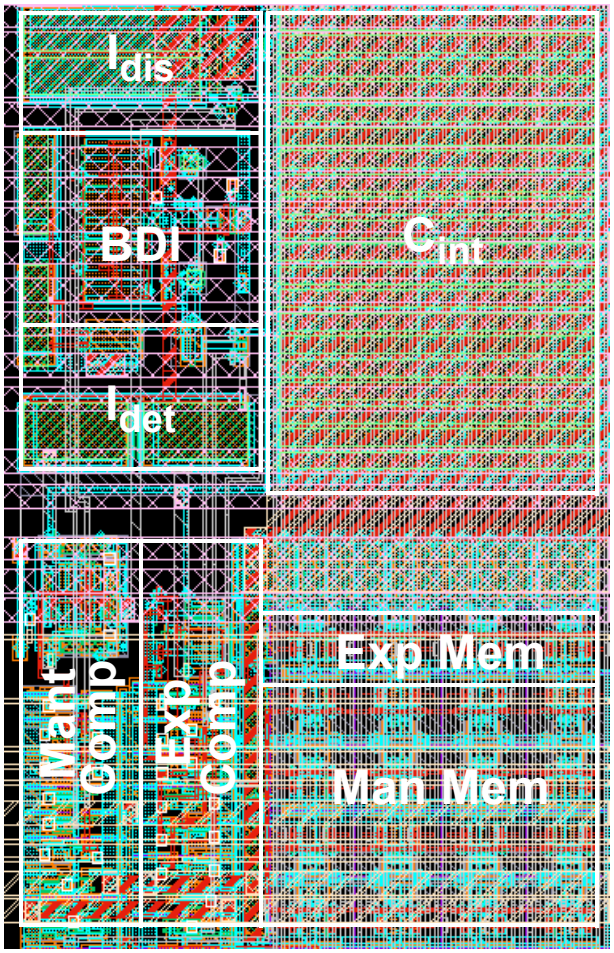


Figure 6.2: Per-pixel ADC layout.

The bottom half of the pixel includes digital circuitry comprising the exponent and mantissa comparators on the left and the digital memory blocks on the right. The digital control signals (metal 4) are routed horizontally above these digital blocks. To reduce the coupling between the analog and the digital circuit regions through the substrate, P and N guard rings are placed between the two regions.

The names of the power supply and current bias pins are listed in Table 6.1 along with their nominal values. The internal circuits use a 1.8-V VDD, and the I/O circuits use a 3.3-V VDD. The analog and digital power supplies are separated, and multiple power planes are used to minimize the coupling of noise between different blocks. The names of the I/O signal pins and their descriptions are listed in Table 6.2.

Power supply	Blocks used	Value
VDDA1, GNDA1	Analog bias, BDI	1.8 V, 0 V
VDDA2	Input mirror cell	3.3 V
GNDA2	Alternate path of detector current	0 V
VDDA3, GNAD3	Mantissa comparator, alternate path of discharge current source	1.8 V, 0 V
VDDA4, GNDA4	Analog output driver	3.3 V, 0 V
VDDD1, GNDD1	Exponent comparator, counters, buffers, memory, digital readout	1.8 V, 0 V
VDDD2, GNDD2	Digital input clocks	1.8 V, 0 V
VDDD3, GNDD3	Digital output driver	1.8 V, 0 V
SUBD	Digital substrate	0 V
I1 (sink)	Analog output driver	200 μA
I2 (source)	BDI PMOS	10 μA
I3 (source)	BDI NMOS	15 μA
I4 (source)	Mantissa Comparator	20 μA

Table 6.1 Power supply and bias of 2-D prototype.

Signal name	Description	in/out
I_{in}<3:1>	detector current for test pixels	in
I_{det}	detector current for regular pixels	in
I_{dis}	discharge current	in
V_{gate}	bias voltage of common gate buffer for test pixels	in
V_{mid}	V_{mid} for exponent comparators	in
V_{low}	V_{low} for mantissa comparators	in
Clk_{Exp}	exponent clock	in
Clk_{Mant}	mantissa clock	in
En_{Exp}	enable exponent clock	in
En_{Mant}	enable mantissa clock	in
Clk_{Row}	clock used to increment row decoder	in
Clk_{Load}	clock used to load data from SRAM into parallel-in/serial-out shift register	in
$Clk_{I/O}$	clock used to transfer data from parallel-in/serial-out shift register to off chip	in
Rd_{Exp}	read exponent memory	in
Rd_{Mant}	read mantissa memory	in
Mode	mode selection for row decoder (increment with Clk_{Row} or not)	in
Reset	power-on reset	in
On_{mid}	turn on V_{mid}	in
On_{dis}	turn on I_{dis}	in
On_{Mant}	turn on mantissa comparator	in
V_{cap}<3:1>	integration capacitor voltage of test pixels	out
Exp<3:1>	exponent of test pixels	out
Mant<3:1>	mantissa of test pixels	out
D<4:0>	digital memory output (D<4> for exponent and D<3:0> for mantissa)	out

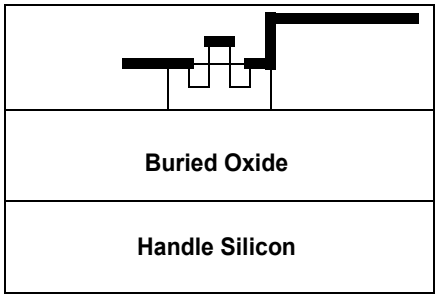
Table 6.2 I/O signals and their descriptions.

6.2 MITLL 3-D FDSOI Technology

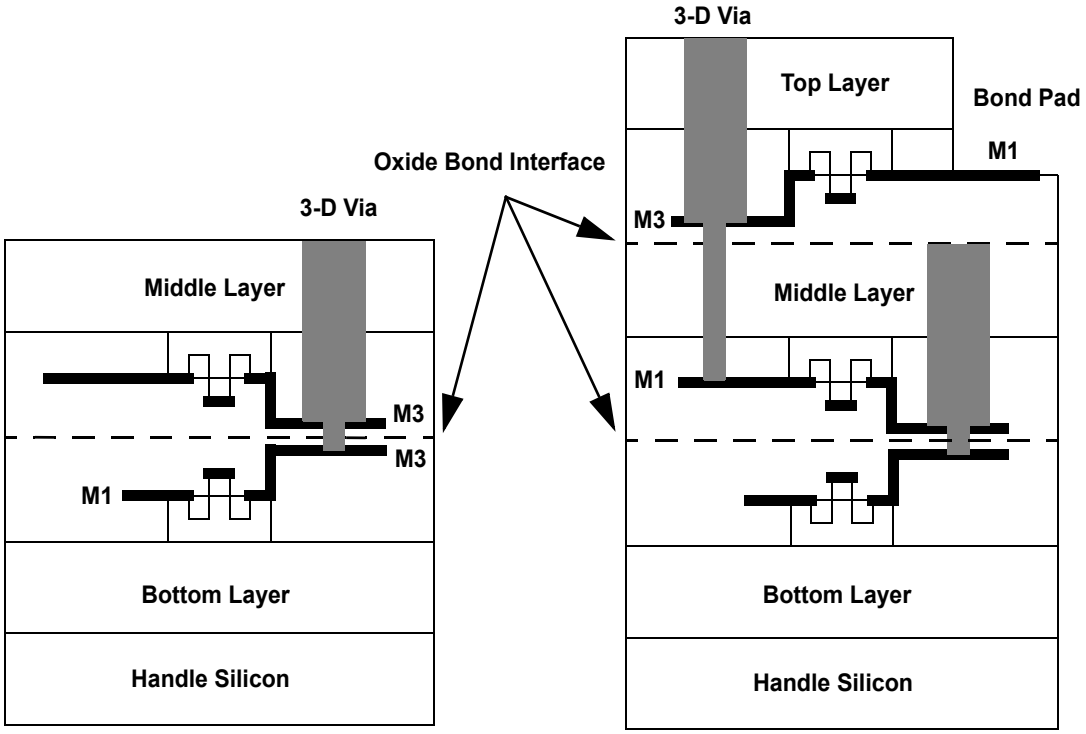
Figure 6.3 illustrates the fabrication steps of the 3-D FDSOI technology of the MIT Lincoln Laboratory (MITLL). Each wafer, with three layers of metal, is fabricated and thinned, after which oxide-to-oxide bonding is used to form the final monolithic 3-D structure. The 3-D vias are formed by etching vertical holes and depositing tungsten in the holes. The bonding pads are formed by etching out the oxide layer of the top wafer. The electrical connection between the bottom layer and the middle layer uses metal 3 and metal 3, whereas the connection between the middle and the top layers uses metal 1 and metal 3. Bonding pads are formed using metal 1 on the top layer. The layout difficulty of aligning the constituent metal layers of 3-D vias (metal 3 and metal 3 between the bottom and middle layers, metal 1 and metal 3 between the middle and top layers) was resolved by using a CAD environment that allows for an overlay view of all the layers.

A vertical cross section of the 3-D FDSOI technology is shown in Figure 6.4. There are three metal layers and one transistor layer in each layer for a total of nine metal layers and three transistor layers in the 3-D chip. The thickness of each layer after thinning is about 7 μm. The through-wafer vias have a diameter and minimum spacing of about 2 μm. The yield of the 3-D via is reported as more than 99.97% [25]. The closest distance between the metals on adjacent layers is about 3μm. Care needs to be taken to minimize signal coupling between such layers.

Since the MITLL 0.18-μm 3-D FDSOI process was still being developed when the 3-D prototype was fabricated, only a preliminary BSIM4 FDSOI HSPICE model was available for the circuit simulations. To achieve a design that is tolerant of process variations, fast and slow corner models were generated by varying the parasitic capacitance and threshold voltage of transistors by ±10% and the gate oxide thickness by ±0.5% from the original HSPICE model and used for the corner simulations.



(a) Fabricate three wafers individually.



(b) Oxide bond second wafer on top of first wafer and form 3-D vias.

(c) Oxide bond third wafer on top of second wafer and form 3-D vias.

Figure 6.3: Fabrication steps of 3-D FDSOI process.

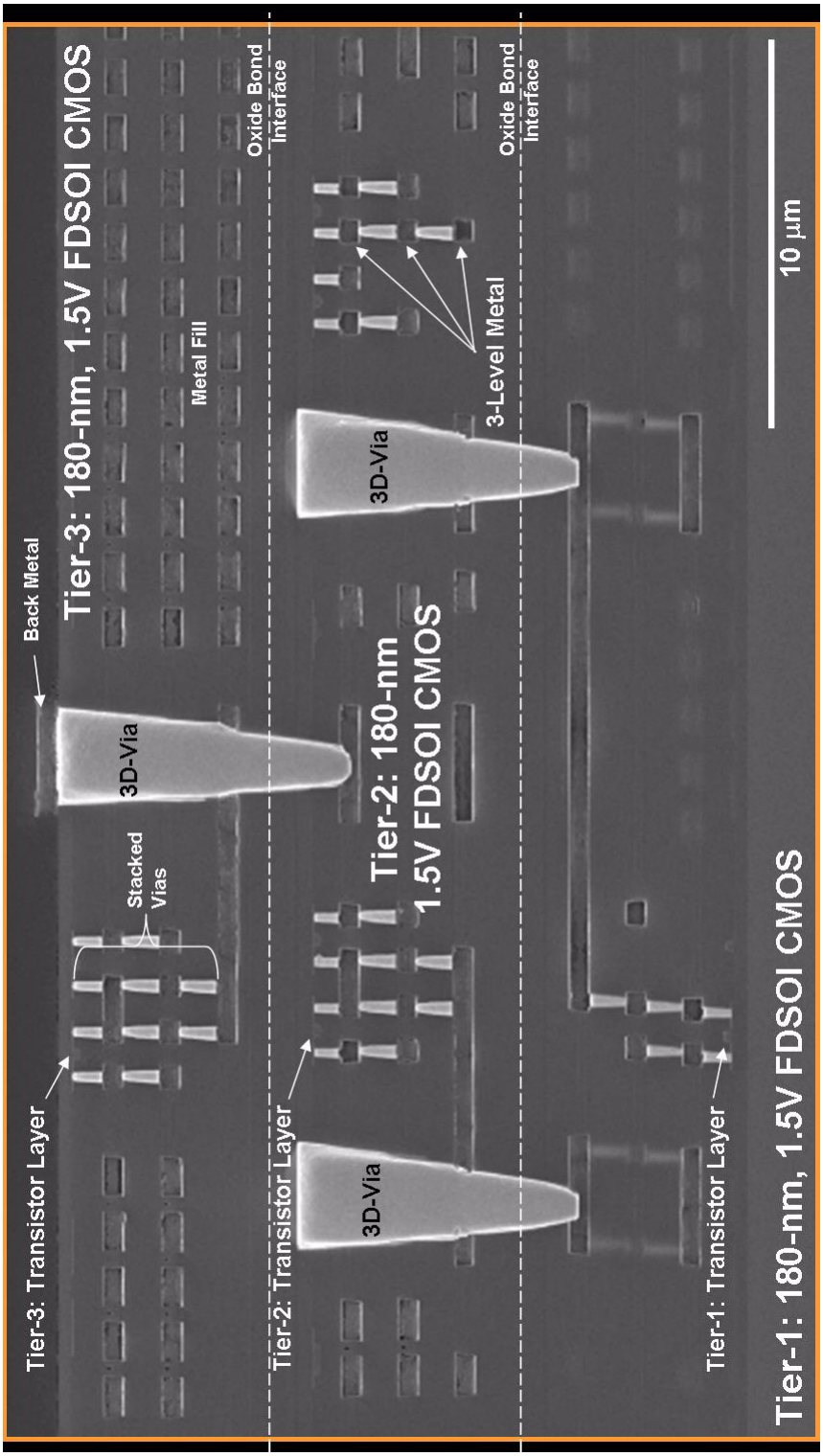


Figure 6.4: Vertical cross section of three layers of 3-D FDSOI (Courtesy of MIT Lincoln Laboratory).

6.3 3-D Prototype in FDSOI

The proposed per-pixel ADC architecture is not only easily scaled to larger array sizes, but also is well-suited to 3-D integration. Figure 6.5 is a micrograph of the 3-D chip. The total chip size is 2.1 x 2.1 mm^2. As depicted in Figure 6.6, the 3-D prototype of the per-pixel ADC is partitioned into three layers to fit within the target LWIR detector size of 50 x 50 μm^2. The use of a per-pixel electronic shutter and a per-pixel ADC makes it easier to connect the partitioned blocks in the 3-D array with a minimum number of vertical interconnections. The 3-D technology imposes tighter constraints on layout than a conventional 2-D process because of the planarization required for wafer-to-wafer oxide bonding. Consequently, to comply with the low density requirement for the polysilicon layer, the integration capacitor is implemented on two layers.

Figure 6.7 shows the physical layout of the three layers of the per-pixel ADC. The top layer contains the PMOS current source, the BDI circuit, part of the integration capacitor, and the exponent comparator. The middle layer contains the remainder of the integration capacitor, the mantissa comparator, and the discharge current source. The bottom layer contains the SRAM blocks. The bottom layer can be further utilized to include a digital signal processing block, such as data selection circuitry to decrease the off-chip data bandwidth. At least two or more 3-D vias were used to make solid signal connections between different layers regardless of 3-D via failures.

The names of the power supply and current bias pins are listed in Table 6.3 along with their nominal values. Similar to the 2-D implementation, the analog and digital power supplies are separated, and multiple power planes are used to minimize the coupling of noise between different blocks. Because the 3-D process employs FDSOI technology, there is no substrate pin. The VDD for internal circuits is 1.5 V, and that for I/O devices is 2.5 V.

The names of the I/O signal pins are the same as those of the 2-D prototype presented in Table 6.2.

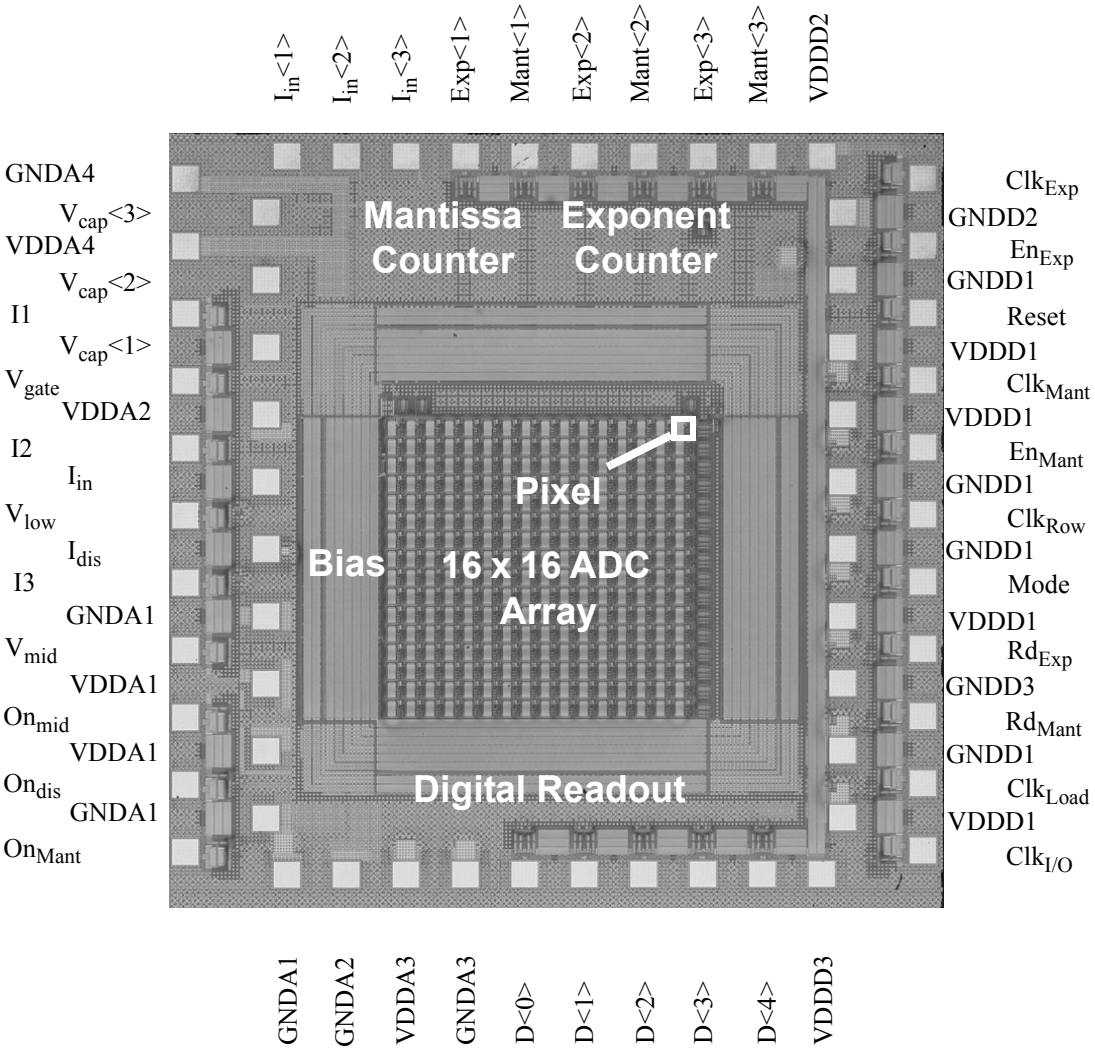


Figure 6.5: 3-D chip micrograph.

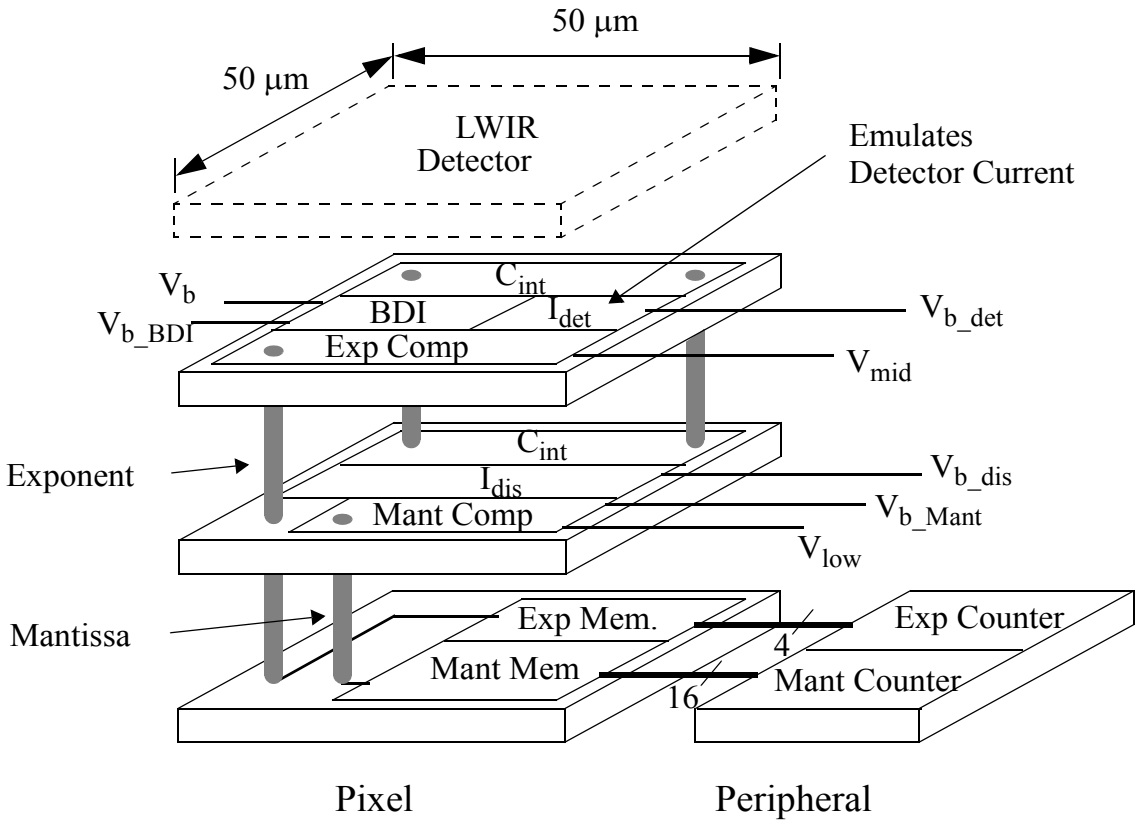


Figure 6.6: Partition of per-pixel ADC into three layers.

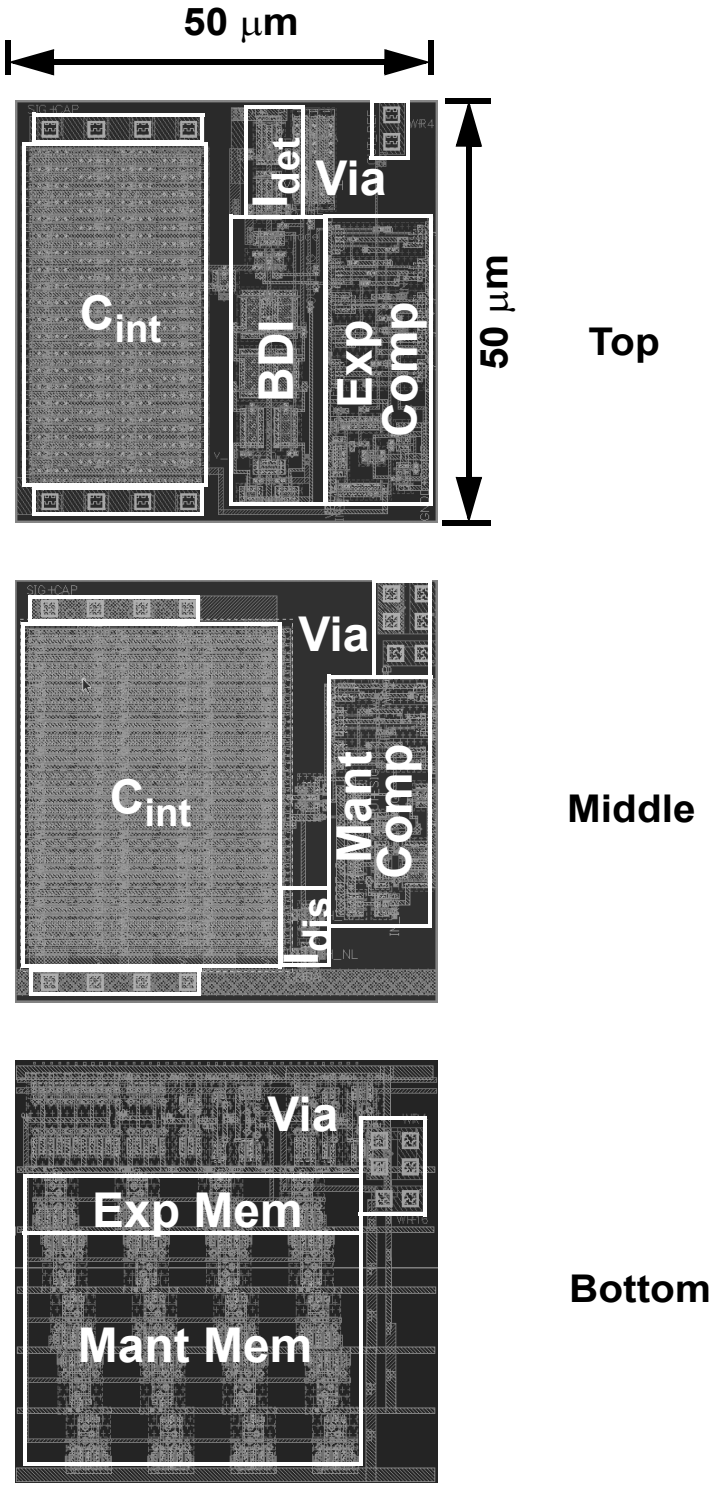


Figure 6.7: Per-pixel ADC layout partitioned into three layers.

Power supply	Blocks used	Value
VDDA1, GNDA1	Analog biases and references, BID	1.5 V, 0 V
VDDA2	Input mirror cell	2.5 V
GNAD2	Alternate path of detector current	0 V
VDDA3, GNAD3	Mantissa comparator, alternate path of discharge current source	1.5 V, 0 V
VDDA4, GNDA4	Analog output driver	2.5 V, 0 V
VDDD1, GNDD1	Exponent comparator, counters, buffers, digital readout	1.5 V, 0 V
VDDD2, GNDD2	Digital input clocks	1.5 V, 0 V
VDDD3, GNDD3	Digital output driver	1.5 V, 0 V
I1 (sink)	Analog output driver	100 μA
I2 (source)	BDI PMOS	20 μA
I3 (source)	Mantissa Comparator	20 μA

Table 6.3 Power supply and bias of 3-D prototype.

6.4 Summary

This chapter describes layout details for the 2-D and 3-D prototypes. As is usual in mixed-signal circuit designs, care has been taken to isolate the digital signals from the sensitive analog blocks in both prototypes. For the 3-D prototype, additional efforts were made to fit the ADC within the LWIR detector size of 50 x 50 μm^2 by partitioning the per-pixel ADC, such that the number of vertical vias connecting the circuit blocks implemented on different layers is minimized.

Chapter 7 *Experimental Results*

This chapter describes the test pixel and the measurement setup designed for the characterization of the per-pixel floating-point dual-slope ADC and then presents the measurement results. For the test pixel, the input current is supplied by an external precision current source, while the voltage of the integration capacitor and the outputs of the exponent and mantissa comparators are monitored directly without using the memory readout circuitry.

Section 7.1 describes the test pixel, and Section 7.2 presents the test setup composed of a printed circuit test board, an FPGA board, and the bench-top test instrumentation. Section 7.3 presents the measured performance of the 2-D and 3-D prototypes.

7.1 Test Pixel

To test the proposed per-pixel ADC, rather than using the pixel with the PMOS cascode current source and the BDI circuit described in Chapter 5, the test pixel shown in Figure 7.1 was designed to supply a precisely known input current (I_{in}) to the ADC via a bonding pad. The test pixel employs a simple PMOS common-gate buffer, rather than BDI, because the large capacitance associated with the bonding pad at the input node of the ADC makes it difficult to stabilize the op-amp in the BDI circuit. Two test pixels are placed next to each other at the top left corner of the 16 x 16 array, and one test pixel is placed at the top right corner in order to measure the mismatch between ADCs at different distances.

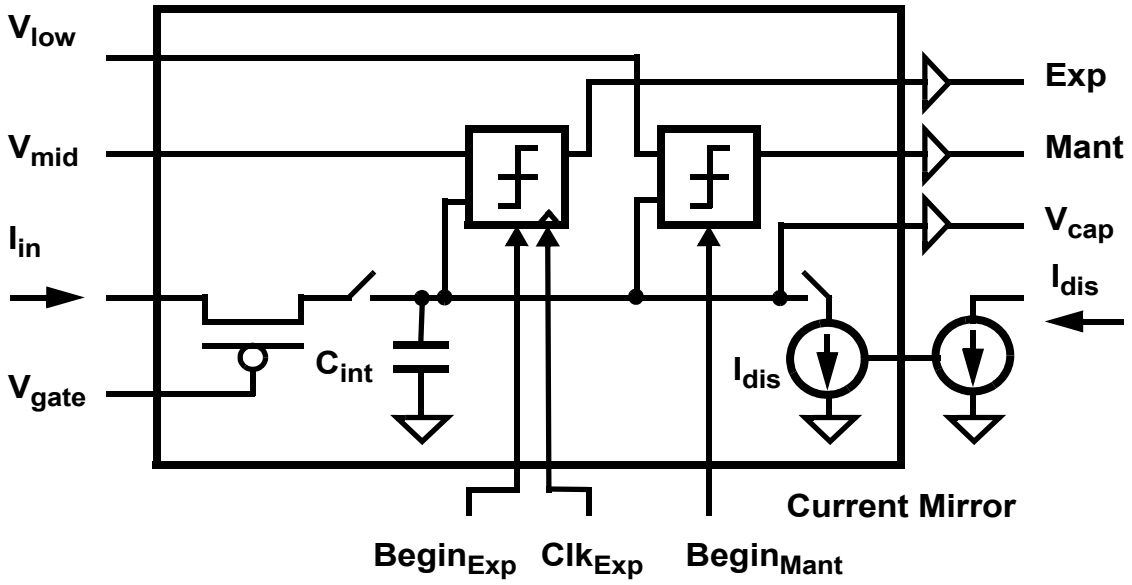


Figure 7.1: Block diagram of test pixel used for ADC characterization.

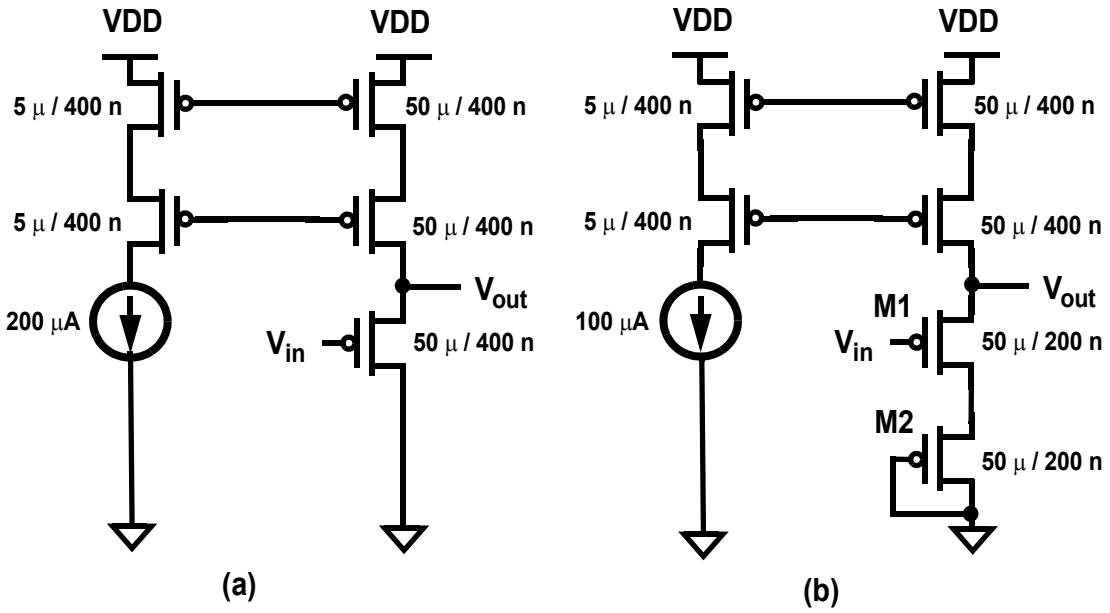


Figure 7.2: Source follower buffers for (a) 2-D prototype and (b) 3-D prototype.

A source follower buffer and two inverter buffers were placed next to the test pixels to monitor the voltage of the integration capacitor and the outputs of the exponent and mantissa comparators, respectively. Figure 7.2 shows schematics of the source follower buffer

as implemented in the 2-D and the 3-D prototypes. Since the I/O devices in the 3-D technology have a lower breakdown voltage than those in the 2-D technology, the diode-connected transistor M2 was placed between the M1 transistor and ground in the 3-D prototype.

7.2 Test Setup

Figure 7.3 shows a picture of the measurement setup used to characterize both the 2-D and 3-D prototypes. Figure 7.4 is a block diagram of the setup. The test setup consists of a prototype ADC chip mounted on a printed circuit board (PCB), a field programmable gate array (FPGA) board, a bench-top precision current source that supplies the input current signals to the ADCs, an HP 8130A pulse generator that generates the mantissa clock for the ADC array and the digital clock for the FPGA board, an oscilloscope that measures the outputs of the ADC, and a computer.

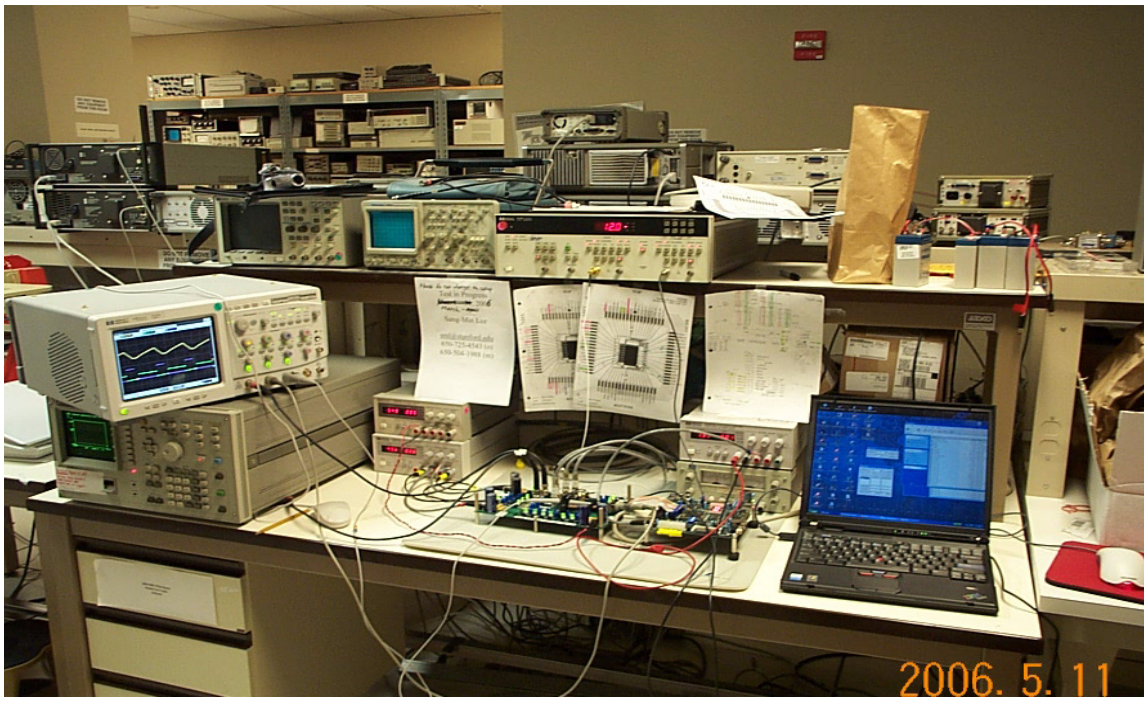


Figure 7.3: Experimental test setup.

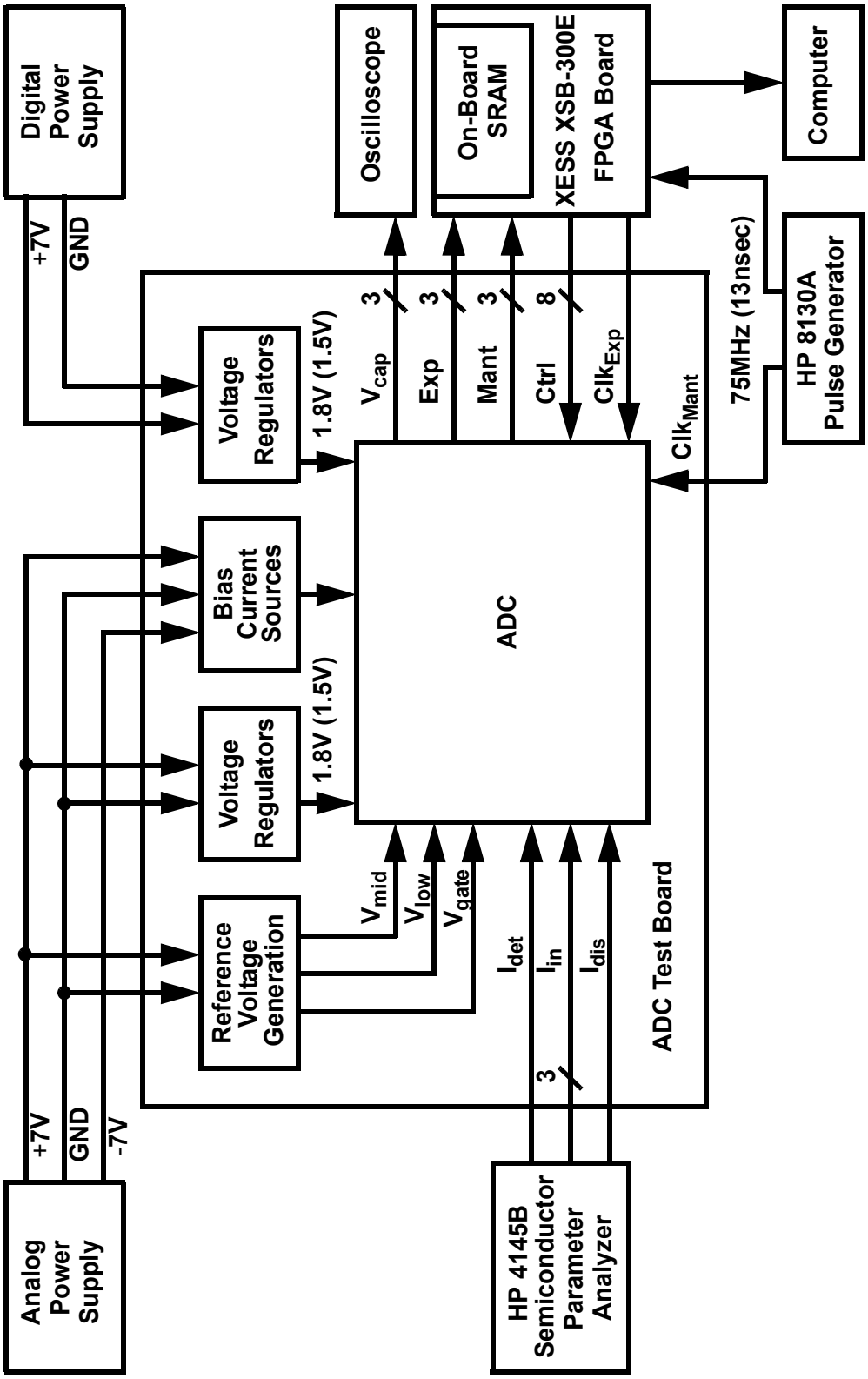


Figure 7.4: Block diagram of experimental test setup.

Both the 2-D and 3-D prototype chips, with test pixels as described above, were packaged in 68-pin, J-lead, ceramic quad flat packages and placed in a surface-mount QFP socket on the test board as shown in Figure 7.5. The FR4 test board employs four copper conductor layers to reduce board noise. The four layers are assigned for signal, ground, power, and signal from the top to the bottom. Separate external power supplies are used to power analog and digital supply domains on the test PCB. Each power supply uses a regulator, and the regulated supply is bypassed with 10-nF, 100-nF, 1-µF, 10-µF, and 100-µF surface-mount chip capacitors close to the socket [54]. Initially, separate ground planes were used for the analog and digital domains to minimize coupling between the two domains. However, a single ground plane was found to be better at reducing the board noise than separate ground planes, which can probably be attributed to smaller return current loops and reduced displacement current in the single ground design.

Adjustable low-dropout (LDO) voltage regulators were used on the ADC test board to supply power to the various power supply domains for the chip. Separate voltage regulators were used to power the adjustable current source integrated circuits (LM334) that provide the bias currents to the master current sources for the BDI circuit, the mantissa

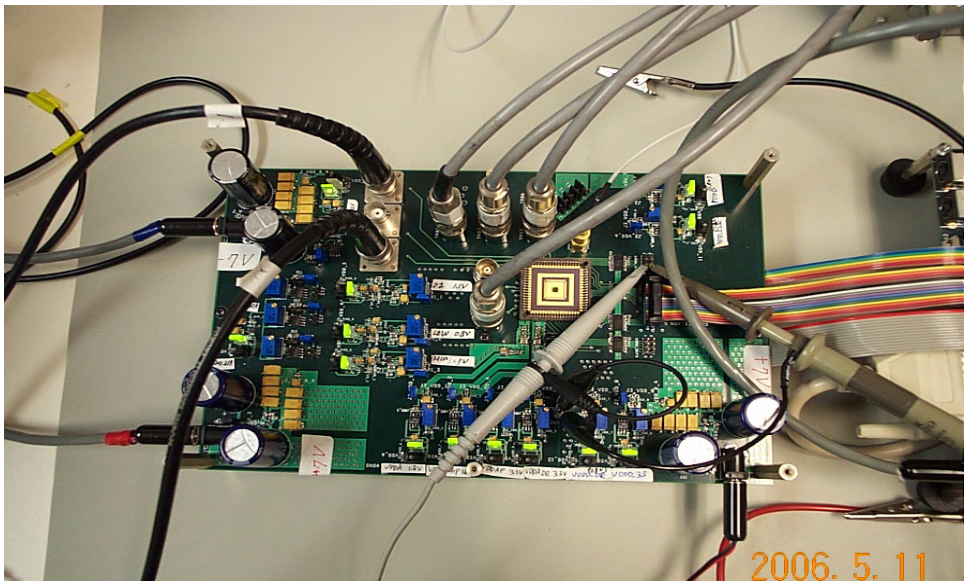


Figure 7.5: Test printed circuit board.

comparator, and the source follower buffer. All power supply and bias lines are bypassed with surface-mount chip capacitors placed near the leads of the socket for the experimental ADC. Reference voltages for the comparators are generated using a voltage regulator and an op-amp. These references are bypassed with 1-nF, 10-nF, 100-nF, 1-μF, and 10-μF surface-mount chip capacitors close to the socket. The op-amp driving the large capacitive load of the PCB trace was compensated for using the techniques presented in [55].

The FPGA (Xilinx Spartan-IIE) is located on a separate PCB (XESS XSB-300E). Ribbon cables are used to transfer digital data from the FPGA board to the ADC test PCB and vice versa. The digital signals from the FPGA have a 3.3-V swing, whereas the digital signals in the ADC have a 1.8-V swing in the 2-D chip and a 1.5-V swing in the 3-D chip. Thus, bidirectional voltage-level translating buffers (SN74AVCH8T245 from Texas Instruments) were used for voltage-level conversion between the FPGA and ADC signal levels. The FPGA board is configured by downloading a Verilog program from the computer. The FPGA board generates the digital control signals necessary for the ADC array, captures the digital outputs of the ADC array, and transfers the data to the computer for further data processing, such as Fourier analysis.

Figure 7.6 illustrates the setting of the integration and discharge phases and the reference voltages that were used for the measurements. The lengths of the integration and discharge phases are controlled by the FPGA board, while the voltage swing on the integration capacitor is set by the reference voltages generated on the test board. The shortest integration time for these measurements was set at 100 nsec and the longest at 200 μsec. The length of the discharge phase was set at 130 μsec (longer than the maximum discharge time with 70 nA) to allow the variation of the discharge current (up to -50% and +100%) to be digitally corrected. The voltage swing was set to 0.8 V.

An HP 4145B semiconductor parameter analyzer supplies precision currents (10-bit resolution) to the three test pixels. Three output ports of the analyzer are used to feed the input currents ranging from 25 nA to 50 μA to the three ADCs individually. A fourth port

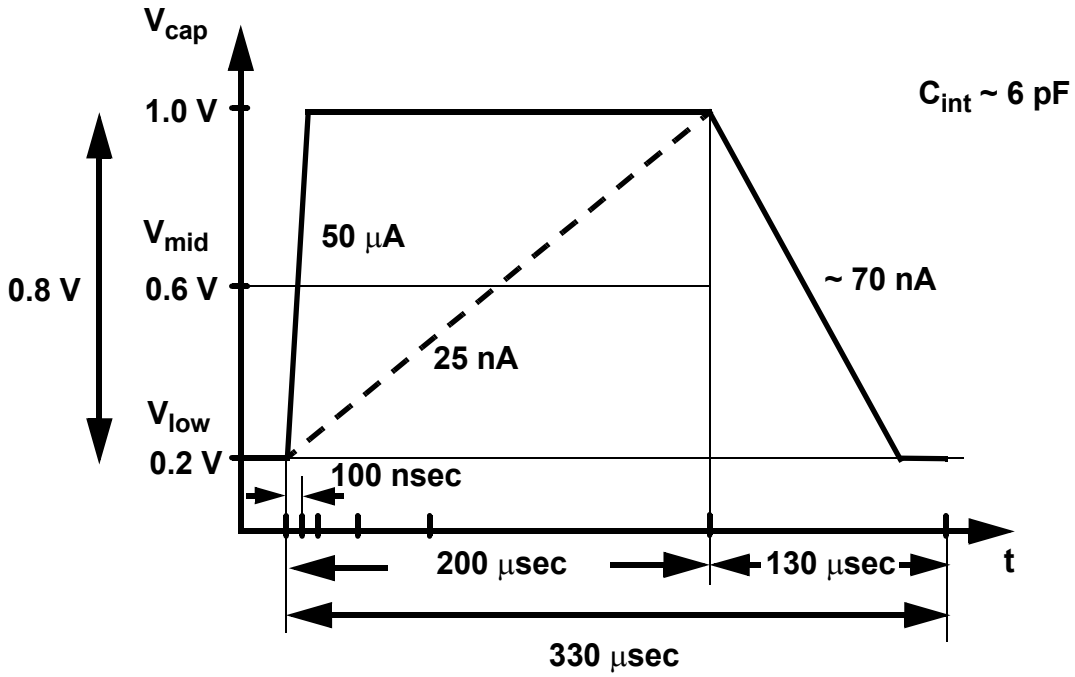


Figure 7.6: Lengths of the integration and discharge phases and the reference voltages used for measurements.

of the equipment is used to feed a 70-nA current to the master current source for the per-pixel discharging current sources.

To connect the current source and the test ADC, a tri-axial cable and a tri-axial PCB mount are used. Since the middle conductor of the tri-axial cable is driven to the same potential as the inner conductor to prevent current leakage to the ground shield, the middle conductor is floating at the PCB side. To minimize the current leakage on the PCB, the tri-axial PCB mounts are placed close to the ADC chip.

Instead of using the counters, memory, and digital readout circuits of the prototype chip, the output of the comparators in the test pixel were fed to the FPGA board. These signals were converted to the exponent and mantissa codes on the FPGA board using the counters and temporary memory implemented in the FPGA chip. Then, the exponent and mantissa codes were transferred to an external 256 k × 16-bit SRAM mounted on the FPGA board. By using the large external SRAM on the FPGA board, we were able to store several hundred frames of the ADC outputs.

7.3 Measured Performance

The 2-D experimental ADC achieves a dynamic range of 19 bits with an 11-bit exponent and an 8-bit mantissa at a 3000-fps frame rate. The automatic selection of the optimal integration time for large and small inputs (50 μA and 25 nA, respectively) is verified in Figure 7.7 and demonstrates the extension of the dynamic range by 11 bits.

Figure 7.8 shows the measured mantissa code variation when a constant detector current of 25 nA is applied. Differences of 100 pA in photocurrents in the range of 25nA were detected, verifying a mantissa resolution of 8 bits. There is a trade-off between the resolution and the frame rate with a fixed integration capacitor size. When the voltage swing and integration time are increased from 0.8 V and 200 μsec to 1.6 V and 400 μsec, respectively, the resolution increases to 9 bits.

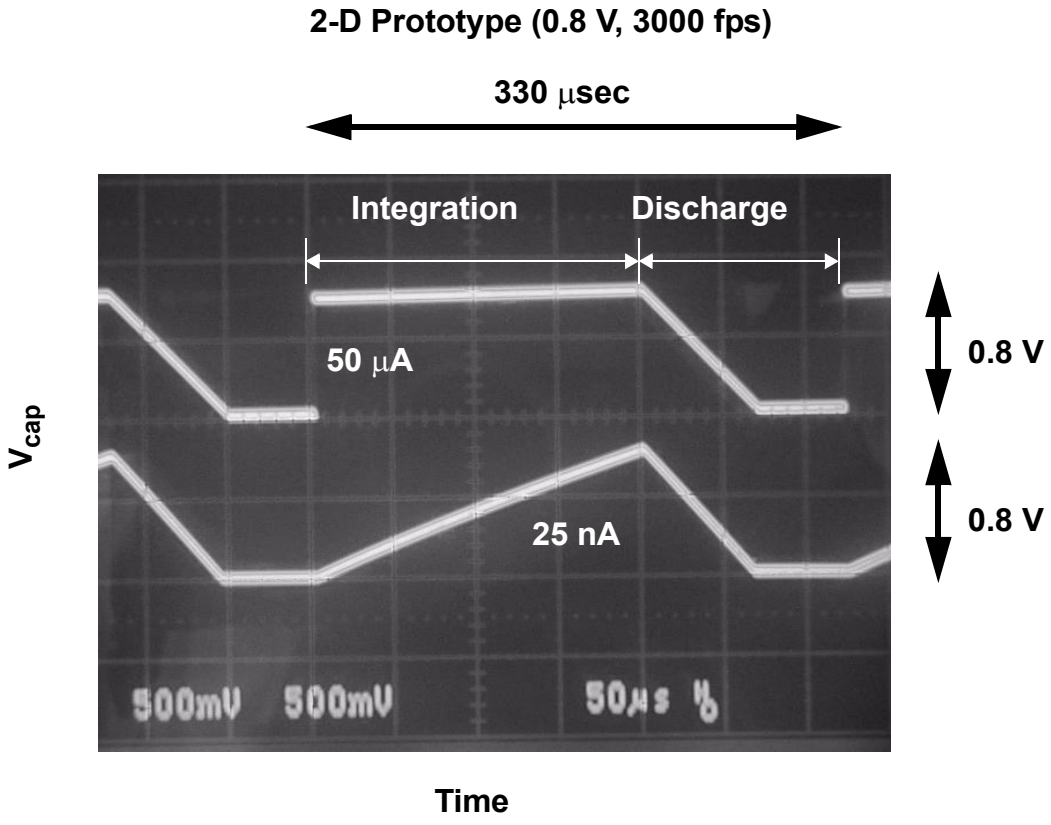


Figure 7.7: Voltage waveforms of the integration capacitor.

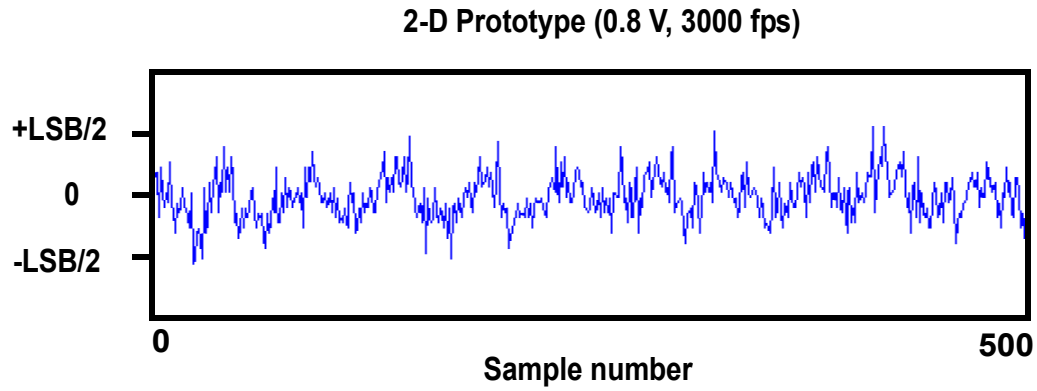


Figure 7.8: Mantissa codes.

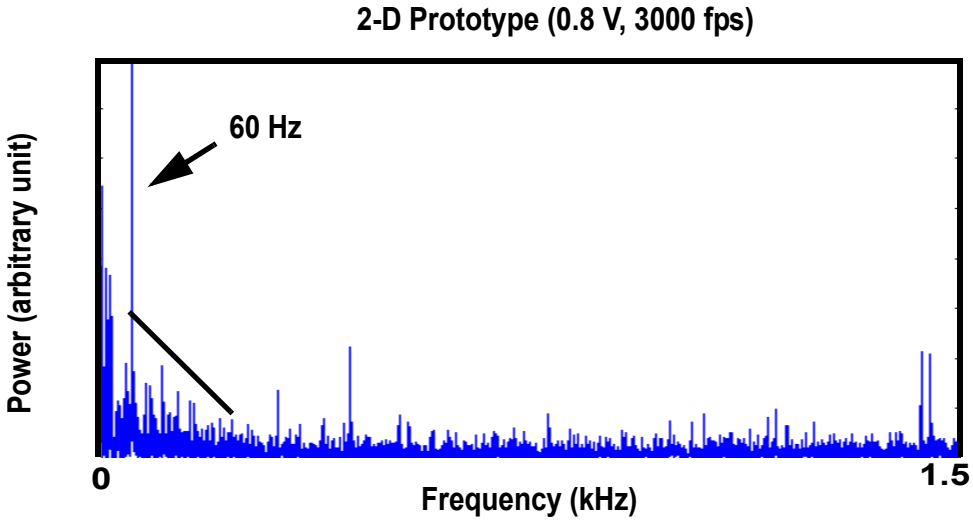


Figure 7.9: FFT of mantissa codes.

A fast Fourier transform (FFT) of the mantissa codes measured for a setting of 25 nA, 0.8 V, and 200 μsec was used to assess the noise spectrum, which is shown in Figure 7.9. From the shape of the spectrum at low frequency and the 60-Hz tone, we observe that the ADC resolution is influenced by 1/f noise both in the mantissa comparator and the current source and board noise coupling into the reference for that comparator. While the offset cancellation removes 1/f noise from DC to 3 kHz, noise above 3 kHz is not cancelled, but is aliased down to the signal band and degrades the resolution.

The variation in gain among the test pixels due to the combined mismatch of the integration capacitances and the discharge current sources was within the design range of -50% and +100% for nine 2-D test pixels and five 3-D test pixels. There was no obvious correlation between the mismatch and the pixel separation distance. Figure 7.10 shows a measured A/D transfer characteristic after the gain correction. The gain correction was performed by adjusting the mantissa code for the 25-nA input current to 255.

The simulated per-pixel ADC power dissipation was 7 μW, which meets a target power budget of 0.5 W for a 256 x 256 array. The BDI circuit dissipates 3.5 μW, the mantissa comparator 2.5μW, and the digital and readout circuits 1 μW.

Table 7.1 summarizes the performance of the 2-D and 3-D experimental prototypes. Note that there is a one bit degradation in resolution between the 2-D and 3-D implementations. This degradation is thought to originate from coupling between the digital counter

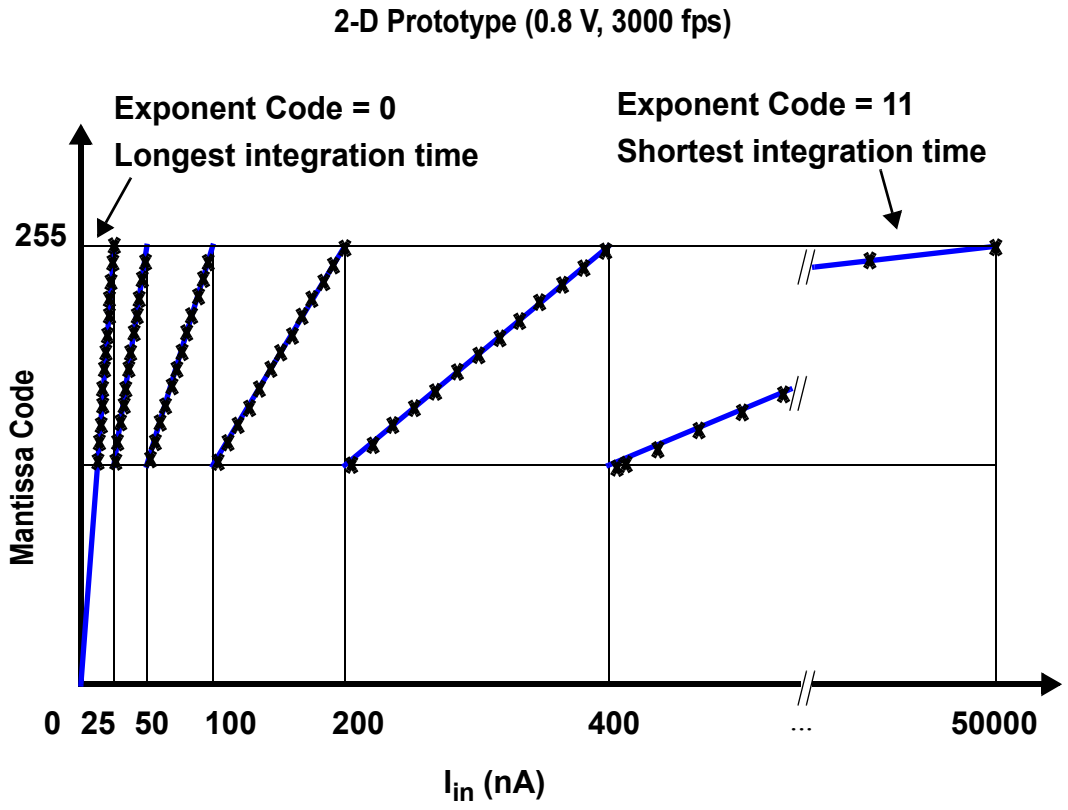


Figure 7.10: ADC transfer characteristic.

routing on the bottom layer and the integration capacitor on the middle layer. The distance between the capacitor on the middle and the digital routing on the bottom layer is about 3 μm, and the digital voltage swing is 1.5V. The metal shield used in the 2-D prototype should have been employed in the 3-D prototype to protect the integration capacitor from the digital signal coupling.

The measurement results demonstrate that the per-pixel floating-point dual-slope ADC architecture is capable of achieving a high frame rate and a high dynamic range for IR FPA applications. In addition, 3-D integration is an effective way to miniaturize the circuit size.

	2-D	3-D
LWIR Detector	HgCdTe (50 x 50 μm^2)	HgCdTe (50 x 50 μm^2)
Integration Capacitor	6 pF	6.5 pF
Array Size	16 x 16	16 x 16
Technology	0.18-μm CMOS 1P5M	0.18-μm FDSOI 1P3M
Supply Voltage	1.8 V	1.5 V
Integration Time (Min, Max)	100 nsec, 200 μsec	100 nsec, 200 μsec
Discharge Time (Max)	130 μsec	130 μsec
Frame Rate	3000 fps	3000 fps
Dynamic Range	19 bits	18 bits
Exponent	11 bits	11 bits
Mantissa Resolution	8 bits @ 0.8-V swing	7 bits @ 0.8-V swing
Per-Pixel Power Dissipation	7 μW	7 μW
ADC Size	50 x 80 μm^2	50 x 50 μm^2 (x 3)

Table 7.1 Performance summary of 2-D and 3-D prototypes.

Chapter 8 *Conclusion*

8.1 Summary

The objective of this work has been to demonstrate a low-power small-area A/D conversion system for high-dynamic range and high-frame rate IR focal plane imaging. A low-power small-area data conversion system is required for IR focal plane imaging because the system must be integrated within the size of an IR detector array, and the total power dissipation is limited by the cooling capacity of the cryogenic cooler used for the focal plane array. However, it is difficult to enhance both the frame rate and dynamic range (DR) with constrained power and area. The conflicting requirements of increasing the frame rate and DR simultaneously with low power dissipation have been achieved with a per-pixel floating-point dual-slope ADC, which is comprised of an electronic shutter and a current-mode dual-slope ADC. In addition, the size of the ADC has been reduced by integrating it in multiple layers using a 3-D IC technology.

A per-pixel ADC approach not only provides the bandwidth needed for high frame rate imaging, but also allows per-pixel DR enhancement necessary for high DR imaging. A floating-point architecture, which lowers the power dissipation of the ADC, has been implemented using an electronic shutter that adjusts the integration time of each pixel adaptive to the strength of input photocurrent. The electronic shutter is controlled by a comparator that monitors the voltage on the integration capacitor. The offset cancellation capability inherent in the dual-slope architecture reduces the offset non-uniformity among the ADCs, which make it easy to correct for gain non-uniformity with multiplication in the digital domain.

Two experimental 16 x 16 ADC arrays have been integrated in a 2-D and 3-D IC technologies. The 2-D prototype was integrated in a 0.18-μm, single-poly, 5-metal CMOS technology with a 1.8-V supply; it achieves a 19-bit DR and 8-bit resolution at 3000 fps, with a power consumption of only 7 μW/pixel. The 3-D prototype was integrated in 0.18-μm, single-poly, 3-metal FDSOI technology with a 1.5-V supply and achieves similar performance. In the 3-D implementation each ADC was partitioned into three layers in order to fit within a pixel size of 50 x 50 μm^2.

8.2 Suggestions for Future Research

As shown in Chapter 5, the thermal noise of the per-pixel current is one of the dominant factors that limit the mantissa resolution of the proposed ADC. The mantissa resolution measured at room temperature (~300 K) is close to the thermal noise level calculated using the thermal noise Equation (5.3).

Operating the ADC at a cryogenic temperature of 70 K would help to reduce the thermal noise voltage by a factor of two. In addition, since this noise voltage is inversely proportional to the capacitance of the integrator, increasing the capacitance also reduces the noise. However, the detector current must be increased proportionally to maintain the same high frame rate. Reducing the discharge time and g_m of the current source simultaneously could reduce the thermal noise of the current source, but this would put the current source deep into subthreshold operation. Therefore, mismatch of the current sources in subthreshold operation needs to be considered during the design.

Another way of increasing the mantissa resolution is to increase the voltage swing on the integration capacitor, which is limited by the breakdown voltage of the technology used for the implementation. Therefore, a high breakdown voltage process would provide better mantissa resolution.

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